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STATUTORY DECLARATION

Kyung Gu KANG, a citizen of the Republic of Korea and a staff member of Y.H.KIM INTERNATIONAL PATENT & LAW OFFICE specializing in "LIQUID CRYSTAL DISPLAY OF HORIZONTAL ELECTRIC FIELD APPLYING TYPE AND FABRICATING METHOD THEREOF" do hereby declare that:

I am conversant with the English and Korean languages and a competent translator thereof.

To the best of my knowledge and belief, the following is a true and correct translation of the Relativity Document (No. P2003-21116) in the Korean language already filed with Korean Industrial Property Office on April 3, 2003.

Signed this 16th day of March, 2006

Kyung Gu KANG

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PATENT APPLICATION

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TITLE OF THE INVENTION: LIQUID CRYSTAL DISPLAY OF HORIZONTAL ELECTRIC FIELD APPLYING TYPE AND FABRICATING METHOD THEREOF

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[ABSTRACTS]

[ABSTRACT]

A liquid crystal display using horizontal electric field and a method of fabricating the liquid crystal display device that are capable of reducing the number of mask processes are provided.

The liquid crystal display of horizontal electric field applying type according to the present invention includes: a gate line; a common line parallel to the gate line; a data line intersected with the gate line and the common line to define a pixel area; a thin film transistor formed on each intersection of the gate line and the data line; a common electrode formed in the pixel area and connected to the common line; a pixel electrode connected to the thin film transistor and formed to produce horizontal electric field along with the common electrode in the pixel area; a gate pad formed with at least one conductive layer included in the gate line; a data pad formed with at least one conductive layer included in the data line; a common pad formed with at least one conductive layer included in the common line; a passivation film for exposing at least any one of the gate pad, the data pad and the common pad; and a driving integrated circuit mounted on a substrate in order to directly connect to any one of the gate pad and the data pad.

[REPRESENTATIVE DRAWING]

Fig. 15

[SPECIFICATION]

[TITLE OF THE INVENTION]

LIQUID CRYSTAL DISPLAY OF HORIZONTAL ELECTRIC FIELD APPLYING TYPE AND FABRICATING METHOD THEREOF

[BRIEF DESCRIPTION OF THE DRAWINGS]

Fig. 1 is a plan view showing the related art thin film transistor array substrate of liquid crystal display of horizontal electric applying type;

Fig. 2 is a sectional view of the thin film transistor array substrate taken along the lines I-I'and II-II' in Fig. 1;

Figs. 3A to 3D are sectional views sequentially illustrating a method of manufacturing the thin film transistor array substrate shown in Fig. 2;

Fig. 4 is a plan view showing a thin film transistor array substrate among the liquid crystal display of horizontal electric applying type according to an embodiment of the present invention;

Fig. 5 is a sectional view of the thin film transistor array substrate taken along the lines III-III'and IV-IV' in Fig. 4;

Fig. 6A and Fig. 6B are a plan view and a sectional view for explaining a first mask process among a manufacturing method of a thin film transistor array substrate according to

the embodiment of the present invention, respectively;

Figs. 7A to 7C are sectional views for concretely explaining the first mask process among the manufacturing method of a thin film transistor array substrate according to the embodiment of the present invention;

Figs. 8A and 8B are a plan view and a sectional view for explaining a second mask process among the manufacturing method of the thin film transistor array substrate according to the embodiment of the present invention, respectively;

Figs. 9A to 9E are sectional views for concretely explaining the second mask process among the manufacturing method of the thin film transistor array substrate according to the embodiment of the present invention;

Figs. 10A and 10B are a plan view and a sectional view for explaining a third mask process among the manufacturing method of the thin film transistor array substrate according to the embodiment of the present invention, respectively;

Figs. 11A to 11C are sectional views for concretely explaining the third mask process among the manufacturing method of the thin film transistor array substrate according to the embodiment of the present invention;

Fig. 12 is a sectional view showing pads of a first structure in the thin film transistor substrate according to the embodiment of the present invention;

Fig. 13 is a sectional view showing pads of a second structure in the thin film transistor substrate according to the embodiment of the present invention;

Fig. 14 is a plan view showing a liquid crystal display having a first structure according to the embodiment of the present invention;

Fig. 15 is a sectional view showing the liquid crystal display shown in Fig. 14;

Fig. 16 is a plan view showing a liquid crystal display having a second structure according to the embodiment of the present invention; and

Fig. 17 is a sectional view showing the liquid crystal display shown in Fig. 16.

<DETAILED DESCRIPTION OF THE REFERENCE NUMERALS>

2, 102: gate line
4, 104: data line
6, 106: thin film transistor
8, 108: gate electrode
10: source electrode
12, 112: drain electrode
13, 27, 33, 39, 127, 133, 139: contact hole
14, 114: pixel electrode
16, 116: common line
18, 118: common electrode
20, 120: storage capacitor
22, 122: storage electrode
24, 124: gate pad
26: gate pad lower electrode

28: gate pad upper electrode

30, 130: data pad

32: data pad lower electrode

34: data pad upper electrode

36, 136: common pad

38: common pad lower electrode

40: common pad upper electrode

42, 142: first gate metal layer

44, 144: second gate metal layer

45, 145: substrate

46, 146: gate insulating film

48, 148: active layer

50, 150: ohmic contact layer

52, 152: passivation film

147: first semiconductor layer

149: second semiconductor layer

154: first source/drain metal layer

156: second source/drain metal layer

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[TECHNICAL FIELD INCLUDING THE INVENTION AND PRIOR ART THEREIN]

The present invention relates to a liquid crystal display using horizontal electric field, and more particularly to a liquid crystal display and a fabricating method thereof that are capable of reducing the number of mask processes.

Generally, liquid crystal displays (LCDs) control light transmittance of liquid crystal material using an electric

field to thereby display a picture. The liquid crystal displays are classified into a vertical electric field type and a horizontal electric field type in accordance with a direction of the electric field driving the liquid crystal.

The liquid crystal display of vertical electric field type, in which a common electrode formed on an upper substrate and a pixel electrode formed on a lower substrate are arranged as facing each other, drives a liquid crystal of a twisted nematic mode (TN) by a vertical electric field formed between the common electrode and the pixel electrode. The liquid crystal display of vertical electric field type has an advantage of a large aperture ratio, while it has a defect of a narrow viewing angle about 90°.

The liquid crystal display of horizontal electric field type drives a liquid crystal of in plane switch (hereinafter referred to as "IPS") mode by a horizontal electric field between the pixel electrode and the common electrode disposed in parallel on the lower substrate. The liquid crystal display of horizontal electric field type has an advantage of an wide viewing angle about 160°. Hereinafter, the liquid crystal display of horizontal electric field type will be described in detail.

The liquid crystal display of the horizontal electric

field type comprises a thin film transistor array substrate and a color filter array substrate as faced and joined each other, a spacer for uniformly maintaining a cell gap between two array substrates and a liquid crystal injected into a space provided by the spacer.

The thin film transistor array substrate includes a plurality of signal lines for forming a horizontal electric field on a basis of a pixel, a plurality of thin film transistors, and an alignment film coated for a liquid crystal alignment thereon. The color filter array substrate includes a color filter for representing a color, a black matrix for preventing a light leakage and an alignment film coated for a liquid crystal alignment thereon.

In such a liquid crystal display, since the thin film transistor array substrate involves a semiconductor process and requires a plurality of mask processes, the manufacturing process is complicate to be a major rise factor in the manufacturing cost of the liquid crystal display panel. In order to solve this, the thin film transistor array substrate has been developed toward a reduction in the number of mask processes. This is because one mask process includes a lot of processes such as thin film deposition, cleaning, photolithography, etching, photo-resist stripping and inspection processes, etc. Recently, there has been highlighted

a four-round mask process in which one mask process is reduced from the existent five-round mask process that is employed as a standard mask process.

Fig. 1 is a plan view illustrating a related art thin film transistor substrate of horizontal electric type using the four-round mask process, and Fig. 2 is a sectional view of the thin film transistor array substrate taken along the I-I' and II-II' line in Fig. 1.

Referring to Figs. 1 and 2, the related art thin film transistor array substrate of horizontal electric type comprises a gate line 2 and a data line 4 formed on a lower substrate 45 in such a manner to intersect each other, a thin film transistor 6 formed at each intersection, a pixel electrode 14 and a common electrode 18 formed in order to apply the horizontal electric field in a pixel regions defined by the intersection and a common line 16 connected to the common electrode 18. Further, the related art thin film transistor array substrate comprises a storage capacitor 20 formed at an overlapped portion between the pixel electrode 14 and the common line 16, a gate pad 24 connected to the gate line 2, and a data pad 30 connected to the data line 4 and a common pad 36 connected to the common line 16.

The gate line 2 supplies a gate signal to the gate

electrode 8 of the thin film transistor 6. The data line 4 supplies a pixel signal to the pixel electrode 14 via a drain electrode 12 of the thin film transistor 6. The gate line 2 and the data line 4 are formed in an intersection structure to thereby define the pixel area 5.

The common line 16 is formed in parallel with the gate line 2 with the pixel area 5 positioned between the common line 16 and the gate line 2 to supply a reference voltage for driving the liquid crystal to the common electrode 18.

The thin film transistor 6 responds to the gate signal of the gate line 2 so that the pixel signal of the data line 4 is charged to the pixel electrode 14. To this end, the thin film transistor 6 comprises a gate electrode 8 connected to the gate line 2, a source electrode 10 connected to the data line 4 and a drain electrode 12 connected to the pixel electrode 14. Further, the thin film transistor 6 includes an active layer 48 overlapping with the gate electrode 8 with a gate insulating film 46 positioned between the thin film transistor 6 and the gate electrode 8 and defining a channel between the source electrode 10 and the drain electrode 12. The active layer 48 is formed to overlap with the data line 4, a data pad lower electrode 32 and a storage electrode 22. On the active layer 48, an ohmic contact layer 50 for making an ohmic contact with the data line 4, the source electrode 10, the drain electrode 12,

the data pad lower electrode 32 and the storage electrode 22 is further formed.

The pixel electrode 14, which is connected to the drain electrode 12 of the thin film transistor 6 via a first contact hole 13 passing through a passivation film 52, is formed in the pixel region 5. Particularly, the pixel electrode 14 comprises a first horizontal part 14A connected to the drain electrode 12 and formed in parallel with adjacent gate line 2 and a second horizontal part 14B formed to overlap with the common line 16 and a finger part 14C formed in parallel with the common electrode 18.

The common electrode 18 is connected to the common line 16 and is formed in the pixel area 5. In addition, the common electrode 18 is formed in parallel with the finger part 14C of the pixel electrode 14 in the pixel area 5.

Accordingly, a horizontal electric field is formed between the pixel electrode 14 to which the pixel signal is supplied via the thin film transistor 6 and the common electrode 18 to which the reference voltage is supplied via the common line 16. Moreover, the horizontal electric field is formed between the finger part 14C of the pixel electrode 14 and the common electrode 18. The liquid crystal molecules arranged in the horizontal direction between the thin film transistor array substrate and the color filter array substrate

by the horizontal electric field becomes to rotate due to a dielectric anisotropy. The light transmittance transmitting the pixel area 5 differs in accordance with a rotation amount of the liquid crystal molecules and thereby the pictures can be represented.

The storage capacitor 20 consists of the common line 16, a storage electrode 22 overlapping with the common line 16 with the gate insulating film 46, the active layer 48 and the ohmic contact layer 50 positioned therebetween, and a pixel electrode 14 connected via a second contact hole 21 passing through the storage electrode 22 and the passivation film 52. The storage capacitor 20 allows a pixel signal charged in the pixel electrode 14 to be maintained stably until the next pixel signal is charged.

The gate line 2 is connected, via the gate pad 24, to a gate driver (not shown). The gate pad 24 consists of a gate pad lower electrode 26 extended from the gate line 2, and a gate pad upper electrode 28 connected, via a third contact hole 27 passing through the gate insulating film 46 and the passivation film 52, to the gate pad lower electrode 26.

The data line 4 is connected, via the data pad 30, to the data driver (not shown). The data pad 30 consists of a data pad lower electrode 32 extended from the data line 4, and a data pad upper electrode 34 connected, via a fourth contact hole 33

passing through the passivation film 52, to the data pad lower electrode 32.

The common line 16 supplied with the reference voltage from the reference voltage source of exterior (not shown) via the common pad 36. The common pad 36 consists of a common pad lower electrode 38 extended from the common line 16, and a common pad upper electrode 40 connected, via a fifth contact hole 39 passing through the gate insulating film 46 and the passivation film 52, to the common pad lower electrode 38.

A method of fabricating the thin film transistor substrate having the above-mentioned structure using the four-round mask process will be described in detail with reference to Figs. 3A to 3D.

Referring to Fig. 3A, a first conductive pattern group including the gate line 2, the gate electrode 8 and the gate pad lower electrode 26 is formed on the lower substrate 45 using the first mask process.

More specifically, a first metal layer 42 and a second metal layer 44 are sequentially formed on the upper substrate 45 by a deposition technique such as a sputtering to form a gate metal layer of double-structure. Then, the gate metal layer is patterned by the photolithography and the etching process using a first mask to thereby form the first conductive pattern group including the gate line 2, the gate electrode 8,

the gate pad lower electrode 26, the common line 16, common electrode 18 and the common pad lower electrode 38. Herein, the first metal layer 42 is formed with an aluminum system metal and the second metal layer 44 is formed with a chrome (Cr) or a molybdenum (Mo).

Referring to Fig. 3B, the gate insulating film 46 is formed on the lower substrate 45 provided with the first conductive pattern group. Further, a semiconductor pattern group including the active layer 48 and the ohmic contact layer 50 and a second conductive pattern group including the data line 4, the source electrode 10, the drain electrode 12, the data pad lower electrode 32 and the storage electrode 22 are formed on the gate insulating film 46 using the second mask process.

More specifically, the gate insulating film 46, a first semiconductor layer, a second semiconductor layer and a data metal layer are sequentially formed on the lower substrate 45 provided with the first conductive pattern group by deposition techniques such as the plasma enhanced chemical vapor deposition (PECVD) and the sputtering, etc. Herein, the gate insulating film 46 is made of an inorganic insulating material such as silicon oxide (SiO_x) or silicon nitride (SiN_x). The first semiconductor layer is made of amorphous silicon that an impurity is not doped and the second conductor layer is made of

amorphous silicon that an impurity of a N type or P type is doped. The data metal layer is made of a molybdenum (Mo), a titanium (Ti), tantalum (Ta) or a molybdenum-alloy, etc.

Then, a photo-resist pattern is formed on the data metal layer by the photolithography using a second mask. In this case, a diffractive exposure mask having a diffractive exposing part at a channel portion of the thin film transistor is used as a second mask, thereby allowing a photo-resist pattern of the channel portion to have a lower height than other photo-resist patterns of area portions.

Subsequently, the data metal layer is patterned by a wet etching process using the other photo-resist patterns to thereby provide the data pattern including the data line 4, the source electrode 10, the drain electrode 12 being integral to the source electrode 10 and the storage electrode 22.

Next, the first semiconductor layer and the second semiconductor layer are patterned at the same time by a dry etching process using the same photo-resist pattern to thereby provide the ohmic contact layer 50 and the active layer 48.

The photo-resist pattern having a relatively low height is removed from the channel portion by the ashing process and thereafter the source electrode, the drain electrode and the ohmic contact layer 50 of the channel portion are etched by the dry etching process. Thus, the active layer 48 of the channel

portion is exposed to separate the source electrode 10 from the drain electrode 12.

Then, a remainder of the photo-resist pattern on the second conductive pattern group is removed using the stripping process.

Referring to Fig. 3C, the passivation film 52 including first to fifth contact holes 13, 21, 27, 33 and 39 are formed on the gate insulating film 46 provided with the second conductive pattern group using the third mask process.

More specifically, the passivation film 52 is entirely formed on the gate insulating film 46 provided with the data pattern by a deposition technique such as the plasma enhanced chemical vapor deposition (PECVD). The passivation film 52 is patterned by the photolithography and the etching process using the third mask to thereby form first to fifth contact holes 13, 21, 27, 33 and 39. The first contact hole 13 is formed in such a manner to pass through the passivation film 52 and exposes the drain electrode 12, whereas the second contact hole 21 is formed in such a manner to pass through the passivation film 52 and exposes the storage electrode 22. The third contact hole 27 is formed in such a manner to pass through the passivation film 52 and the gate insulating film 46 and exposes the gate pad lower electrode 26, whereas the fourth contact hole 33 is formed in such a manner to pass through the passsivation film

52 and exposes the data pad lower electrode 32, and the fifth contact hole 39 is formed in such a manner to pass through the passivation film 52 and the gate insulating film 46 and exposes the common pad lower electrode 38. Herein, when a metal which has high ratio of dry etching like a molybdenum (Mo) is used for the data metal, the first contact hole 13, the second contact hole 21 and the forth contact hole 33 are formed in such a manner to pass through to the drain electrode 12, the storage electrode 22 and the data pad lower electrode 32, respectively, to thereby expose their side.

The passivaion film 52 is made of an inorganic insulating material such as the gate insulating film 46 or an organic insulating material having a small dielectric constant such as an acrylic organic compound, BCB (benzocyclobutene) or PFCB (perfluorocyclobutane), etc.

Referring to Fig. 3D, a third conductive pattern group including the pixel electrode 14, the gate pad upper electrode 28, the data pad upper electrode 34 and the common pad upper electrode 40 is formed on the passivation film 52 using the fourth mask process.

More specifically, a transparent conductive film is coated onto the passivation film 52 by a deposition technique such as the sputtering, etc. Then, the transparent conductive film is patterned by the photolithography and the etching

process using a fourth mask, to thereby provide the third conductive pattern group including the pixel electrode 14, the gate pad upper electrode 28, the data pad upper electrode 34 and the common pad upper electrode 40. The pixel electrode 14 is electrically connected, via the first contact hole 13, to the drain electrode 12 while being electrically connected, via the second contact hole 21, to the storage electrode 22. The gate pad upper electrode 28 is electrically connected, via the third contact hole 37, to the gate pad lower electrode 26. The data pad upper electrode 34 is electrically connected, via the fourth contact hole 33, to the data pad lower electrode 32. The common pad upper electrode 40 is electrically connected, via the fifth contact hole 39, to the common pad lower electrode 38.

In this connection, the transparent conductive film may be made of an indium-tin-oxide (ITO), a tin-oxide (TO), an indium-zinc-oxide (IZO) or an indium tin zinc oxide (ITZO).

As described above, the related art thin film transistor array substrate of horizontal electric field type and the manufacturing method thereof adopts a four-round mask process, thereby reducing the number of manufacturing processes in comparison to the five-round mask process and hence reducing a manufacturing cost to that extent. However, since the four-round mask process also still has a complex manufacturing process and a limit in reducing a cost, there has been required

an approach that is capable of more simplifying the manufacturing process and more reducing the manufacturing cost.

[TECHNICAL SUBJECT MATTER TO BE SOLVED BY THE INVENTION]

Accordingly, it is an object of the present invention to provide a liquid crystal display using horizontal electric field and a method of fabricating a liquid crystal display device that is capable of reducing the number of mask processes.

[CONFIGURATION AND OPERATION OF THE INVENTION]

In order to achieve these and other objects of the invention, the liquid crystal display of horizontal electric field applying type according to the present invention comprises: a gate line; a common line parallel to the gate line; a data line intersected with the gate line and the common line to define a pixel area; a thin film transistor formed on each intersection of the gate line and the data line; a common electrode formed in the pixel area and connected to the common line; a pixel electrode connected to the thin film transistor and formed to produce horizontal electric field along with the common electrode in the pixel area; a gate pad formed with at least one conductive layer included in the gate line; a data pad formed with at least one conductive layer included in the data line; a common pad formed with at least one conductive

layer included in the common line; a passivation film for exposing at least any one of the gate pad, the data pad and the common pad; and a driving integrated circuit mounted on a substrate in order to directly connect to any one of the gate pad and the data pad.

The driving integrated circuit includes a gate driving integrated circuit directly connected to the gate pad.

The driving integrated circuit further includes a data driving integrated circuit directly connected to the data pad.

The driving integrated circuit further includes a data driving integrated circuit connected to the data pad using a conductive film.

The liquid crystal display of horizontal electric field applying type further comprises a signal supplying line for supplying a driving signal to the driving integrated circuit.

Each of the gate line and the common line includes a main conductive layer and a subsidiary conductive layer for providing against an opening of the main conductive layer.

Each of the gate pad and the common pad comprise the main conductive layer and the subsidiary conductive layer, and wherein the subsidiary conductive layer has an exposed structure.

Each of the gate pad and the common pad comprises a subsidiary conductive layer.

The data line comprises a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

The data pad includes the main conductive layer and the subsidiary conductive layer, and wherein the subsidiary conductive layer has an exposed structure.

The data pad includes the subsidiary conductive layer.

The main conductive layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten which are a low resistance metal; and the subsidiary conductive layer includes a titanium.

The thin film transistor comprises: a gate electrode connected to the gate line; a source electrode connected to the data line; a drain electrode opposite to the source electrode; and a semiconductor layer for forming a channel between the source electrode and the drain electrode.

The drain electrode and the pixel electrode are made of an identical conductive layer.

The semiconductor layer is formed on the gate insulating film along the data line, the source electrode, the drain electrode and the pixel electrode.

In order to achieve these and other objects of the invention, a method for fabricating a liquid crystal display of horizontal electric field applying type includes: preparing a

thin film transistor array substrate having a gate line and a data line, a thin film transistor formed at an intersection of the gate line and the data line, a pixel electrode connected to the thin film transistor, a common electrode producing horizontal electric field along with the pixel electrode and a common line connected to the common electrode and wherein the thin film transistor array substrate has a structure in which any one of a gate pad formed with at least one conductive layer included in the gate line, a data pad formed with at least one conductive layer included in the data line and a common pad formed with at least one conductive layer included in the common line is exposed through a passivation film; and mounting the driving integrated circuit on the substrate so that any one of the exposed gate pad and the data pad is directly connected to the driving integrated circuit.

The step of mounting the driving integrated circuit on the substrate includes mounting the gate driving integrated circuit on the substrate in order to directly connect the gate pad with the gate driving integrated circuit.

The step of mounting the driving integrated circuit on the substrate further includes mounting the data driving integrated circuit on the substrate in order to directly connect the data pad with the data driving integrated circuit.

The step of mounting the driving integrated circuit on

the substrate further includes connecting the data pad with the data driving integrated circuit using a conductive film.

The step of preparing a thin film transistor array substrate includes: forming, on a substrate, a first conductive pattern group including the gate line, a gate electrode connected to the gate line, the common line parallel to the gate line, the common electrode, the gate pad and the common pad; forming a gate insulating film on the substrate having the first conductive pattern group thereon; forming a semiconductor layer at a predetermined area of the gate insulating film and a second conductive pattern group having the date line, a source electrode of the thin film transistor connected with the data line, a drain electrode of the thin film transistor being opposite to the source electrode, a pixel electrode connected with the drain electrode and paralleled to the common electrode and the data pad; and forming a passivation film for exposing the gate pad, the data pad and the common pad on the gate insulation film having the second conductive pattern group and the semiconductor layer formed thereon.

The first conductive pattern group is formed to have a double-layer structure having a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

The step of forming the passivation film includes

exposing the subsidiary conductive layers of the gate pad and the common pad.

The step of forming the passivation film includes forming a contact hole passing through the passivation film and the gate insulating film to expose the subsidiary conductive layers.

The second conductive pattern group is formed to have a double-layer structure having a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

The step of forming the passivation film includes exposing the subsidiary conductive layer of the data pad.

The step of forming the passivation film includes forming a contact hole passing through the passivation film to expose the subsidiary conductive layer.

The step of forming the passivation film includes forming a contact hole passing through the passivation film and the main metal layer of the data pad to expose the subsidiary conductive layer.

The main conductive layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten which are a low resistance metal, and wherein the subsidiary conductive layer includes a titanium.

These and other objects of the invention will be apparent from the following detailed description of the embodiments of

the present invention with reference to the accompanying drawings, in which:

Hereinafter, the preferred embodiments of the present invention will be described in detail with reference to Figs. 4 to 17.

Fig. 4 is a plan view showing a thin film transistor array substrate of the liquid crystal display of horizontal electric field applying type according to an embodiment of the present invention, and Fig. 5 is a sectional view of the thin film transistor array substrate taken along the lines III-III' and IV-IV' in Fig. 4.

As shown in Figs. 4 and 5, the thin film transistor array substrate comprises a gate line 102 and a data line 104, which have a gate insulating film 146 therebetween, formed on a lower substrate 145 in such a manner to intersect each other, a thin film transistor 106 formed at each intersection of the gate line 102 and the data line 104, a pixel electrode 114 and a common electrode 118 formed in order to apply the horizontal electric field in a pixel region defined by the interconnection and a common line 116 connected to the common electrode 118. Further, the thin film transistor array substrate comprises a storage capacitor 120 formed at an overlapped portion between a upper storage electrode 122 and the common line 116, a gate pad

124 extended from the gate line 102, and a data pad 130 extended form data line 104 and a common pad 136 extended from the common line 116.

The gate line 102 for supplying a gate signal and the data line 104 for supplying a data signal are formed in an intersection structure to thereby define a pixel area 105.

The common line 116 supplying a reference voltage for driving the liquid crystal is formed in parallel with the gate line 102 with the pixel area 105 positioned between the common line 116 and the gate line 102.

The thin film transistor 106 responds to the gate signal of the gate line 102 so that the pixel signal of the data line 104 is charged and maintained in the pixel electrode 114. To this end, the thin film transistor 106 comprises a gate electrode 108 connected to the gate line 102, a source electrode included in the data line 104 and a drain electrode 112 connected to the pixel electrode 114. Further, the thin film transistor 106 includes an active layer 148 overlapping with the gate electrode 108 with having a gate insulating film 146 positioned therebetween and defining a channel between the source electrode and the drain electrode 112.

The active layer 148 is formed to overlap with the data line 104, the data pad 130 and an upper storage electrode 122. On the active layer 148, an ohmic contact layer 150 for making

an ohmic contact with the data line 104, the drain electrode 112, the data pad 130 and the upper storage electrode 122 is further provided.

The pixel electrode 114 being integral to the drain electrode 112 of the thin film transistor 106 and the upper storage electrode 122 is formed in the pixel region 105. Particularly, the pixel electrode 114 comprises a horizontal part 114A extended in parallel with adjacent gate line 102 from the drain electrode 112 and a finger part 114B extended from the horizontal part 114A in vertical direction.

The common electrode 118 is connected to the common line 116 and is formed in the pixel area 105. Specially, the common electrode 118 is formed in parallel with the finger part 114B of the pixel electrode 114 in the pixel area 105.

Accordingly, a horizontal electric field is formed between the pixel electrode 114 to which the pixel signal is supplied via the thin film transistor 106 and the common electrode 118 to which the reference voltage is supplied via the common line 116. Specially, the horizontal electric field is formed between the finger part 14B of the pixel electrode 114 and the common electrode 118. The liquid crystal molecules arranged in the horizontal direction between the thin film transistor array substrate and the color filter array substrate by the horizontal electric field becomes to rotate due to a

dielectric anisotropy. Further, the light transmittance transmitting the pixel area 105 differs in accordance with a rotation amount of the liquid crystal molecules and thereby the pictures can be represented.

The storage capacitor 120 consists of the common line 116 and the upper storage electrode 122 overlapping with the common line 116 with the gate insulating film 146, the active layer 148 and the ohmic contact layer 150 therebetween and being integral with the pixel electrode 114. The storage capacitor 120 allows a pixel signal charged in the pixel electrode 114 to be maintained stably until the next pixel signal is charged.

The gate line 102 is connected, via the gate pad 124, to a gate driver integrated circuit(IC)(not shown) mounted on a tape carried package (TCP). The gate pad 124 is extended from the gate line 102 and is exposed through a first contact hole 127 passing through a gate insulating film 146 and a passivation film 152. The gate pad 124 has an exposed structure of metal layer that has a relatively high strength and corrosion resistance such as a titanium (Ti) and a tungsten (W) included in the gate line 102.

The common line 116 is supplied with the reference voltage from the power source of exterior (not shown) via the common pad 136. The common pad 136 is extended from the common line 116 and is exposed through a third contact hole 127

passing through a gate insulating film 146 and a passivation film 152. The common pad 136 has an exposed structure of metal layer such as a titanium (Ti) and a tungsten (W) as similar as a gate pad 124.

More specifically, the gate line 102, the gate electrode 108, the common line 116 and common electrode 118 have a double-layer structure of metal layers with a first and a second metal layer 142 and 144. Among the metal layers, a metal layer is made of any metal that has a relatively high strength and corrosion resistance such as a titanium (Ti) and a tungsten (W). Whereas, another metal layer is made of a low resistance metal such as an aluminum (Al) system metal, a molybdenum (Mo) and a copper (Cu) that are conventionally employed as a gate metal.

In this connection, in case where the first metal layer 142 is made of any metal that has a high strength and corrosion resistance, the gate pad 124 and the common pad 138 have an exposed structure in which the second metal layer 144 of an upper portion is removed and the first metal layer 142 of the lower portion is exposed. On the other hand, in case where the second metal layer 144 is made of any metal that has a high strength and corrosion resistance, the gate pad 124 and the common pad 138 have an exposed structure in which the second metal layer 144 of an upper portion is exposed.

The data line 104 is connected to a data driver IC (not shown) mounted on a TCP via the data pad 130. The data pad 130 is extended from the data line 104 and is exposed through a second contact hole 133 passing through a passivation film 152. The data pad 130 has an exposed structure of the metal layer that has a relatively high strength and corrosion resistance such as titanium (Ti) and tungsten (W) included in the data line 104. The data pad 130 of metal layer is connected to the TCP in which the data drive IC mounted thereon via antistrophic conductive film (ACF) having a conductive ball. Accordingly, although the process of attaching the data pad 130 and the TCP is performed repeatedly, there does not occur the defect caused by the opening of the data pad 130.

More specifically, the data line 104, the drain electrode 112, the pixel electrode 114 and the upper storage electrode 122 have a double-layer structure of metal layers stacked with a first and a second metal layers 154 and 156. One metal layer of the metal layers is made of any metal that has a relatively high strength and corrosion resistance such as a titanium (Ti) and a tungsten (W). Whereas, another metal layer is made of a low resistance metal such as an aluminum (Al) system metal, a molybdenum (Mo) and a copper (Cu) that are generally employed as a gate metal.

In this connection, in case where the first metal layer

154 is made of any metal having a high strength and corrosion resistance, the data pad 130 has an exposed structure in which the second metal layer 156 of an upper portion is removed and the first metal layer 154 of a lower portion is exposed. On the other hand, in case where the second metal layer 156 is made of any metal having a high strength and corrosion resistance, the data pad 130 has an exposed structure in which the second metal layer 156 of an upper portion is exposed.

Figs. 6A and 6B are a plan view and a sectional view for explaining a first mask process among a manufacturing method of the thin film transistor array substrate of horizontal electric applying type shown in Figs. 4 and 5, respectively.

As shown in Figs. 6A and 6B, a first conductive pattern group including the gate line 102, the gate electrode 108 and the gate pad 124, the common line 116, the common electrode 118 and the common pad 136 is formed on the lower substrate 145 using the first mask process. There will be explained the first mask process in detail with reference to Figs. 7A to 7C.

A first gate metal layer 142 and a second gate metal layer 144 are sequentially formed on the upper substrate 145 by a deposition method such as a sputtering, to thereby a gate metal layer of double-layer structure as shown in Fig. 7A. Herein, any one of the first gate metal layer 142 and the second gate metal layer 144 is made of any metal that has a

relatively high strength and corrosion resistance such as a titanium (Ti) and a tungsten (W), whereas another metal layer is made of a metal such as an aluminum (Al) system metal, a molybdenum (Mo) and a copper (Cu). And then, a photo-resist film is entirely formed on the second gate metal layer 144 and then a first mask 300 is arranged on the lower substrate 145 as shown in Fig. 7B. The first mask 300 comprises a mask substrate 304 which is a transparent material and a cut-off part formed on a cut-off region P2 of the mask substrate 304. Herein, an exposed region in which the mask substrate 304 is exposed becomes an exposure region P1. The photo-resist film is exposed and developed using the first mask 300 as set forth above, to thereby form the photo-resist pattern 306 in the cut-off region P2 corresponding to the cut-off part 302 of the first mask 300. The first and the second gate metal layer 142 and 144 are patterned by an etching process using the photo-resist pattern 306, to thereby form the first conductive pattern group including the gate line, the gate electrode 108, the gate pad 124, the common line 116, the common electrode 118 and the common pad 136.

Figs. 8A and 8B are a plan view and a sectional view for explaining a second mask process among the manufacturing method of the thin film transistor array substrate of horizontal electric applying type according to the embodiment of the

present invention, respectively.

At first, a gate insulating film 146 is formed on the lower substrate 145 provided with the first conductive pattern group by deposition method such as the plasma enhanced chemical vapor deposition (PECVD) or sputtering. The gate insulating film 146 is made of an inorganic insulating material such as silicon oxide (SiO_x) or silicon nitride (SiN_x).

Further, as shown in Figs. 8A and 8B, a semiconductor pattern group including an active layer 148 and the ohmic contact layer 150 and a second conductive pattern group including the data line 104, the drain electrode 112, the pixel electrode 114, the data pad 130 and the upper storage electrode 122 are formed on the gate insulating film 146 using the second mask process. There will be explained the second mask process in detail with reference to Figs. 9A to 9E.

As shown in Fig. 9A, on the gate insulating film 146, a first semiconductor layer 147, a second semiconductor layer 149, a first and a second source/drain metal layer 154 and 156 are sequentially provided by deposition techniques such as the plasma enhanced chemical vapor deposition (PECVD) and the sputtering, etc. Herein, the first semiconductor layer 147 is made of amorphous silicon that an impurity is not doped and the second conductor layer 149 is made of amorphous silicon that an impurity of a N type or P type is doped. Any one of the first

and the second source/drain metal layers 154 and 156 is made of any metal that has a relatively high strength and corrosion resistance such as a titanium (Ti) and a tungsten (W), whereas another metal layer is made of any metal such as an aluminum (Al) system metal, a molybdenum (Mo) and a copper (Cu).

Thereafter, a photo-resist film is formed on the second source/drain metal layer 156 and then a second mask 160 used for a partial exposure is arranged on the lower substrate 145 as shown in Fig. 9B. The second mask 160 comprises a mask substrate 162 which is a transparent material, a cut-off part 164 formed on a cut-off region P2 of the mask substrate 162 and a diffractive exposure part 166 (or a semi-transmitting part) formed on a partial exposure region P3 of the mask substrate 162. Herein, a region in which the mask substrate 162 is exposed becomes an exposure region P1. The photo-resist film is exposed and then developed using the second mask 160 as set forth above, to thereby form the photo-resist pattern 168 which has a stepped part in the cut-off region P2 and the partial exposure region P3 corresponding to the diffractive exposure part 166 and cut-off part 164 of the second mask 160. That is, the photo-resist pattern 168 formed in the partial exposure region P3 has a second height H2 that is lower than a first height H1 of the photo-resist pattern 168 formed to the cut-off region P2.

Subsequently, the first and the second source/drain metal layer 154 and 156 are patterned by a wet etching process using the photo-resist pattern 168, so that the second conductive pattern group including the data line 104, the drain electrode 112 being integral to the source electrode connected to the data line 104, the pixel data 114, the upper storage electrode 122 and the data pad 130 is formed as shown in Fig. 9C.

Further, the first semiconductor layer 147 and the second semiconductor layer 149 are patterned by a dry etching process using the photo-resist pattern 168 as a mask to thereby provide the ohmic contact layer 150 and the active layer 148 along the second conductive pattern group as shown in Fig. 9D. Next, the photo-resist pattern 168 formed with the second height H2 in the partial exposure region P3 is removed by the ashing process using an oxygen (O_2) plasma, whereas the photo-resist pattern 168 formed with the first height H1 in the cut-off region P2 has a lowered height. The partial exposure region P3 by etching process using the photo-resist pattern 168, that is, the first and the second source/drain metal layers 154 and 156 formed at channel portion of the thin film transistor are removed. For instance, in case where the second source/drain metal layer 156 is made of molybdenum Mo and the first source/drain metal layer 154 is made of titanium Ti, the second source/drain metal layer 156 is removed in the channel portion by a dry etching process

and the first source/drain metal layer 154 is removed by a wet etching process in the channel portion. On the contrary, in case where the second source/drain metal layer 156 is made of titanium Ti and the first source/drain metal layer 154 is made of molybdenum Mo, the second source/drain metal layer 156 is removed by a wet etching process in the channel portion and the first source/drain metal layer 154 is removed by a dry etching process in the channel portion. Accordingly, the drain electrode 112 is separated from the data line 104 including the source electrode. Thereafter, the ohmic contact layer 150 is removed by a dry etching process using the photo-resist pattern 168 to thereby expose the active layer 148.

Further, the photo-resist pattern 168 left on the second conductive pattern group is removed by a stripping process as shown in Fig. 9E.

Figs. 10A and 10B are a plan view and a sectional view for explaining a third mask process among the manufacturing method of the thin film transistor array substrate according to the embodiment of the present invention, respectively.

The passivation film 152 including first to third contact holes 127, 133 and 139 is formed on the gate insulating film 146 stacked with the semiconductor pattern and a second conductive pattern group by the third mask process as shown in Figs. 10A and 10B. There will be explained the third mask

process in detail with reference to Figs. 11A to 11C.

The passivation film 152 is formed by a deposition technique such as the plasma enhanced chemical vapor deposition (PECVD) on the gate insulating film 146 where semiconductor pattern and a second source/drain conductive pattern group are stacked. The passivation film 152 is made of an inorganic material such as the gate insulating film 146 or an organic material having a small dielectric constant such as an acrylic organic compound, BCB (benzocyclobutene) or PFCB (perfluorocyclobutane), etc. Subsequently, the photo-resist film is entirely formed on the passivation film 152 and the third mask 310 is arranged on the lower substrate 145 as shown in Fig. 11B. The third mask 310 comprises a mask substrate 314 which is a transparent material, a cut-off part 312 formed on a cut-off region P2 of the mask substrate 314. Herein, a region in which the mask substrate 314 is exposed becomes an exposure region P1. The photo-resist film is exposed and then developed using the third mask 310 to thereby form the photo-resist pattern 316 in the cut-off region P2 depending on cut-off part 312 of the third mask 310. The passivation film 152 is patterned by the etching process using the photo-resist pattern 316 to thereby form the first to the third contact holes 127, 133 and 139.

The first contact hole 127 is formed in such a manner to

pass through the passivation film 152 and the gate insulating film 146 and exposes the gate pad 124, the second contact hole 133 is formed in such a manner to pass through the passivation film 152 and exposes the data pad 130, and the third contact hole 139 is formed in such a manner to pass through the passivation film 152 and the gate insulating film 146 and exposes the common pad 136. The exposed gate pad 124, the data pad 130 and the common pad 136 have an exposed structure of metal that has a high strength and corrosion resistance. In this case, the gate pad 124, the data pad 130 and the common pad 136 have two structures as shown in Figs. 12 and 13.

For example, in case where the first gate metal layer 142 of a lower portion is made of a titanium Ti and the second gate metal layer 144 of an upper portion is made of a molybdenum Mo, the gate pad 124 and the common pad 136 are consisted of only the first gate metal layer 142 of the lower portion as shown in Fig. 12. This is because the second gate metal layer 144 of the upper portion is removed for the etching process employed to form the first and the third contact hole 127 and 139.

On the contrary, in case where the first gate metal layer 142 of the lower portion is made of a molybdenum Mo and the second gate metal layer 144 of the upper portion is made of a titanium Ti, the gate pad 124 and the common pad 136 have a double-layer structure of metal layers in which the first and

the second gate metal layers 142 and 144 are stacked as shown in Fig. 13. Also, the gate pad 124 and the common pad 136 have an exposed structure of the gate metal layer 144 of the upper portion through the use of the first and the third contact hole 127 and 139.

Further, in case where the first source/drain metal layer 154 of the lower portion is made of a titanium Ti and the second source/drain metal layer 156 of the upper portion is made of a molybdenum Mo, the data pad 130 is consisted of only the first source/drain metal layer 154 of the lower portion as shown in Fig. 12. This is because the second source/drain metal layer 156 is removed for the etching process employed to form the second contact hole 133.

On the contrary, in case where the first source/drain metal layer 154 of the lower portion is made of a molybdenum Mo and the second source/drain metal layer 156 is made of a titanium Ti, the data pad 130 has a double-layer structure of metal layers in which the first and the second source/drain metal layers 154 and 156 are stacked as shown in Fig. 13. Also, the data pad 130 has an exposed structure of the source/drain metal layer 156 of the upper portion through the use of the second contact hole 133.

As described above, in the thin film transistor array substrate of horizontal electric applying type and the

fabricating method thereof according to the embodiment of the present invention, the pixel electrode 114 is formed with an identical metal to the drain electrode 112. Further, the gate pad 124, the data pad 130 and the common pad 136 use metal that has a high strength and corrosion resistance enough to prevent the defect caused by the opening of the pad irrespective of the repeated process of attaching the TCP. Accordingly, a transparent conductive film is free in the present invention, that is, the process including the transparent conductive film deposition process and patterning process is unnecessary, which leads to reduce one mask process. In other words, the thin film transistor array substrate of horizontal electric applying type according to the present invention is formed using the three-round mask process.

The thin film transistor array substrate formed using the three-round mask process and the color filter array substrate formed using separate process are prepared and combined and then a liquid crystal is injected therebetween, to thereby fabricate a liquid panel. In this case, the color filter array substrate is combined with the thin film transistor array substrate to expose a pad region where the gate pad, the data pad and the common pad are formed on the thin film transistor array substrate.

Fig. 14 is a plan view representing a liquid crystal

display according to the present invention, and Fig. 15 is a sectional view representing the liquid crystal display shown in Fig. 14.

Referring to Figs. 14 and 15, the liquid crystal display according to the present invention comprises a gate drive IC 264 mounted on a lower substrate 145 of a liquid crystal panel 208 and a data drive IC 272 mounted on a TCP 180.

The gate drive ICs 264 mounted by a COG (a Chip on Glass) system is connected, via the gate pad 124, to the gate lines 102. In other words, an input terminal of the gate drive ICs 264 is connected, via an input bump, to a signal supplying line 274, and an output terminal of the gate drive ICs 264 is connected, via an output bump 260, to the gate pad 124. Such gate drive ICs 264 supplies, via the gate pads, the gate signal to the gate line 102.

For the sake of it, gate control signals and power source signals from timing controller and a power source portion (not shown) on a PCB (a Printed Circuit Board) 270 are supplied to a signal supplying line 274 via the data TCP 180. The signal supplying line 274 is connected to an input terminal of the gate drive ICs 264 through an input bump and supplies the gate control signals and the power source signals to the gate drive IC 264. The gate drive IC 264 makes a gate-driving signal using the gate control signals and the power source signals. The gate

driving signals are supplied to the gate pad 124 through an output bump 260 connected to output terminals 262 of the gate drive IC 264.

The data drive ICs 272 is mounted by a TAB (a Tape Automated Bonding) system on the TCP 180 and are connected to data lines 104 via a data pad 130. That is, the TCP 180, which the data drive ICs 272 are mounted, is attached using an ACF (an Antistrophic Conductive Film) 182 including a conductive ball 184 on a data pad region. Accordingly, output pads 176 formed on a base film 172 of the TCP 180 are electrically connected to the data pad 130, via the ACF 182. Further any one of dummy output pads 178 formed on the base film 172 of the TCP 180 on which the data drive ICs 272 are mounted is electrically connected to the common pad 136 via the ACF 182.

Fig. 16 is a plan view representing other types of a liquid crystal display according to the present invention and Fig. 17 is a sectional view representing the liquid crystal display shown in Fig. 16.

Referring to Figs. 16 and 17, the liquid crystal display according to the present invention comprises a gate drive IC 264 and a data drive IC 272 mounted on a lower substrate 145 of a liquid crystal panel 208 and a FPC (a Flexible Printed Circuit) 180 for supplying a driving signal to the gate drive IC 264 and the data drive IC 272.

The data drive ICs 272 mounted by a COG (a Chip on Glass) system is connected, via the data pad 130, to the data lines 104. In other words, an input terminal of the data drive ICs 272 is connected, via an input bump, to the signal supplying line 274, and an output terminal 284 of the data drive ICs 272 is connected, via an output bump 286, to the data pad 130. Such data drive ICs 272 supplies, via the gate pads, the gate signal to the data line 104.

For the sake of it, data control signals and data signals from timing controller and a power source portion not shown on a PCB 270 are supplied to a signal supplying line 274 via the FPC 280 and a COG connector 288. The signal supplying line 274 is connected to an input terminal of the data drive ICs 272 through an input bump and supplies the data control signals and the data signals to the data drive IC 272. The data drive IC 272 makes a data-driving signal using the data control signals and the data signals. The data driving signals are supplied to the data pad 130 through the output terminals 284 of the data drive IC 272.

The gate drive ICs 264 mounted by a COG (a Chip on Glass) system is connected, via the gate pad 124, to the gate lines 102. In other words, an input terminal of the gate drive ICs 264 is connected, via an input bump, to a signal supplying line 274, and an output terminal of the gate drive ICs 264 is

connected, via an output bump 260, to the gate pad 124. Such gate drive ICs 264 supplies, via the gate pads, the gate signal to the gate line 102.

For the sake of such, gate control signals and power source signals from timing controller and a power source portion not shown on PCB 270 are supplied to a signal supplying line 274 via the FPC 280 and the COG connector 288. The signal supplying line 274 is connected to an input terminal of the gate drive ICs 264 through an input bump and supplies the gate control signals and the power source signals to the gate drive IC 264. The gate drive IC 264 makes a gate-driving signal using the gate control signals and the power source signals. The gate driving signals are supplied to the gate pad 124 through the output terminals 262 of the gate drive IC 264.

The FPC 280 supplies gate control signals and power source signals from timing controller and a power source portion to its corresponding drive ICs 264 and 272. That is, input pad of the FPC is connected to the PCB 279 and output pad of the FPC 280 is connected to the COG connector 288 of the signal supplying line 274.

Further, any one of output pad 282 of the FPC 280 is connected to the common pad 130 using the ACF 182 including the conductive ball 184 and supplies reference voltage for driving liquid crystal to the common line 118.

As mentioned above, any one of the gate drive IC 264 and the data drive IC 272 is mounted by the COG system on the lower substrate such that corrosion of exposed metal layer in the exposed gate pad 124, the exposed data pad 130 and the common pad 136 is prevented.

[EFFECT OF THE INVENTION]

As described above, in the thin film transistor array substrate of horizontal electric field applying type and the manufacturing method thereof according to the present invention, the pixel electrode is formed as an identical metal to the drain electrode, and the pads have the structure wherein a metal layer having a high strength and corrosion resistance is exposed in order to prevent the defect caused by the opening. Accordingly, according to the thin film transistor array substrate of horizontal electric field applying type and the fabricating method thereof according to the present invention, it is possible to manufacture the thin film transistor array substrate using the three-round mask process and therefore to simplify the structure and processes the thin film transistor array substrate, to thereby reduce the manufacturing cost and improve the manufacture yield.

Further, the liquid crystal display of horizontal electric applying type and the manufacturing method thereof

according to the second embodiment of the present invention are capable of preventing the corrosion of metal layer of an exposed pad due to a drive IC is mounted by COG system directly on a substrate.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display of horizontal electric field applying type, comprising:

a gate line;

a common line parallel to the gate line;

a data line intersected with the gate line and the common line to define a pixel area;

a thin film transistor formed on each intersection of the gate line and the data line;

a common electrode formed in the pixel area and connected to the common line;

a pixel electrode connected to the thin film transistor and formed to produce horizontal electric field along with the common electrode in the pixel area;

a gate pad formed with at least one conductive layer included in the gate line;

a data pad formed with at least one conductive layer included in the data line;

a common pad formed with at least one conductive layer included in the common line;

a passivation film for exposing at least any one of the gate pad, the data pad and the common pad; and

a driving integrated circuit mounted on a substrate in order to directly connect to any one of the gate pad and the data pad.

2. The liquid crystal display of horizontal electric field applying type according to claim 1, wherein the driving integrated circuit includes a gate driving integrated circuit directly connected to the gate pad.

3. The liquid crystal display of horizontal electric field applying type according to claim 2, wherein the driving

integrated circuit further includes a data driving integrated circuit directly connected to the data pad.

4. The liquid crystal display of horizontal electric field applying type according to claim 2, wherein the driving integrated circuit further includes a data driving integrated circuit connected to the data pad using a conductive film.

5. The liquid crystal display of horizontal electric field applying type according to claim 1, wherein the liquid crystal display of horizontal electric field applying type further comprises a signal supplying line for supplying a driving signal to the driving integrated circuit.

6. The liquid crystal display of horizontal electric field applying type according to claim 1, wherein each of the gate line and the common line includes a main conductive layer and a subsidiary conductive layer for providing against an opening of the main conductive layer.

7. The liquid crystal display of horizontal electric field applying type according to claim 6, wherein each of the gate pad and the common pad comprise the main conductive layer and the subsidiary conductive layer, and wherein the subsidiary

conductive layer has an exposed structure.

8. The liquid crystal display of horizontal electric field applying type according to claim 6, wherein each of the gate pad and the common pad comprises the subsidiary conductive layer.

9. The liquid crystal display of horizontal electric field applying type according to claim 1, wherein the data line comprises a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

10. The liquid crystal display of horizontal electric field applying type according to claim 9, wherein the data pad includes the main conductive layer and the subsidiary conductive layer, and wherein the subsidiary conductive layer has an exposed structure.

11. The liquid crystal display of horizontal electric field applying type according to claim 9, wherein the data pad includes the subsidiary conductive layer.

12. The liquid crystal display of horizontal electric field

applying type according to any one of claim 6 and claim 9, wherein the main conductive layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten which are a low resistance metal; and

wherein the subsidiary conductive layer includes a titanium.

13. The liquid crystal display of horizontal electric field applying type according to claim 1, wherein the thin film transistor comprising:

a gate electrode connected to the gate line;

a source electrode connected to the data line;

a drain electrode opposite to the source electrode; and

a semiconductor layer overlapped with having the gate electrode and the gate insulating film and for forming a channel between the source electrode and the drain electrode.

14. The liquid crystal display of horizontal electric field applying type according to claim 13, wherein the drain electrode and the pixel electrode are made of an identical conductive layer.

15. The liquid crystal display of horizontal electric field applying type according to claim 13, wherein the semiconductor

layer is formed on the gate insulating film along the data line, the source electrode, the drain electrode and the pixel electrode.

16. A method for fabricating a liquid crystal display of horizontal electric field applying type, which comprises:

preparing a thin film transistor array substrate having a gate line and a data line, a thin film transistor formed at an intersection of the gate line and the data line, a pixel electrode connected to the thin film transistor, a common electrode producing horizontal electric field along with the pixel electrode and a common line connected to the common electrode and wherein the thin film transistor array substrate has a structure in which any one of a gate pad formed with at least one conductive layer included in the gate line, a data pad formed with at least one conductive layer included in the data line and a common pad formed with at least one conductive layer included in the common line is exposed through a passivation film; and

mounting the driving integrated circuit on the substrate so that any one of the exposed gate pad and the data pad is directly connected to the driving integrated circuit.

17. The method according to claim 16, wherein the step of

mounting the driving integrated circuit on the substrate includes mounting the gate driving integrated circuit on the substrate in order to directly connect the gate pad with the gate driving integrated circuit.

18. The method according to claim 17, wherein the step of mounting the driving integrated circuit on the substrate further includes mounting the data driving integrated circuit on the substrate in order to directly connect the data pad with the data driving integrated circuit.

19. The method according to claim 17, wherein the step of mounting the driving integrated circuit on the substrate further includes connecting the data pad with the data driving integrated circuit using a conductive film.

20. The method according to claim 16, wherein the step of preparing a thin film transistor array substrate includes:

forming, on a substrate, a first conductive pattern group including the gate line, a gate electrode connected to the gate line, the common line parallel to the gate line, the common electrode, the gate pad and the common pad;

forming a gate insulating film on the substrate having the first conductive pattern group thereon;

forming a semiconductor layer at a predetermined area of the gate insulating film and a second conductive pattern group having the date line, a source electrode of the thin film transistor connected with the data line, a drain electrode of the thin film transistor being opposite to the source electrode, a pixel electrode connected with the drain electrode and paralleled to the common electrode and the data pad; and

forming a passivation film for exposing the gate pad, the data pad and the common pad on the gate insulation film having the second conductive pattern group and the semiconductor layer formed thereon.

21. The method according to claim 20, wherein the first conductive pattern group is formed to have a double-layer structure having a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

22. The method according to claim 21, wherein the step of forming the passivation film includes exposing the subsidiary conductive layers of the gate pad and the common pad.

23. The method according to claim 21, wherein the step of forming the passivation film includes forming a contact hole

passing through the passivation film and the gate insulating film to expose the subsidiary conductive layers.

24. The method according to claim 21, wherein the step of forming the passivation film includes forming a contact hole passing through the passivation film, the gate insulation film and the main metal layer to expose the subsidiary conductive layers.

25. The method according to claim 20, wherein the second conductive pattern group is formed to have a double-layer structure having a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

26. The method according to claim 25, wherein the step of forming the passivation film includes exposing the subsidiary conductive layer of the data pad.

27. The method according to claim 25, wherein the step of forming the passivation film includes forming a contact hole passing through the passivation film to expose the subsidiary conductive layer.

28. The method according to claim 25, wherein the step of forming the passivation film includes forming a contact hole passing through the passivation film and the main metal layer of the data pad to expose the subsidiary conductive layer.

29. The method according to any one of claim 20 and claim 25, wherein the main conductive layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten which are a low resistance metal, and

wherein the subsidiary conductive layer includes a titanium.

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FIG.1

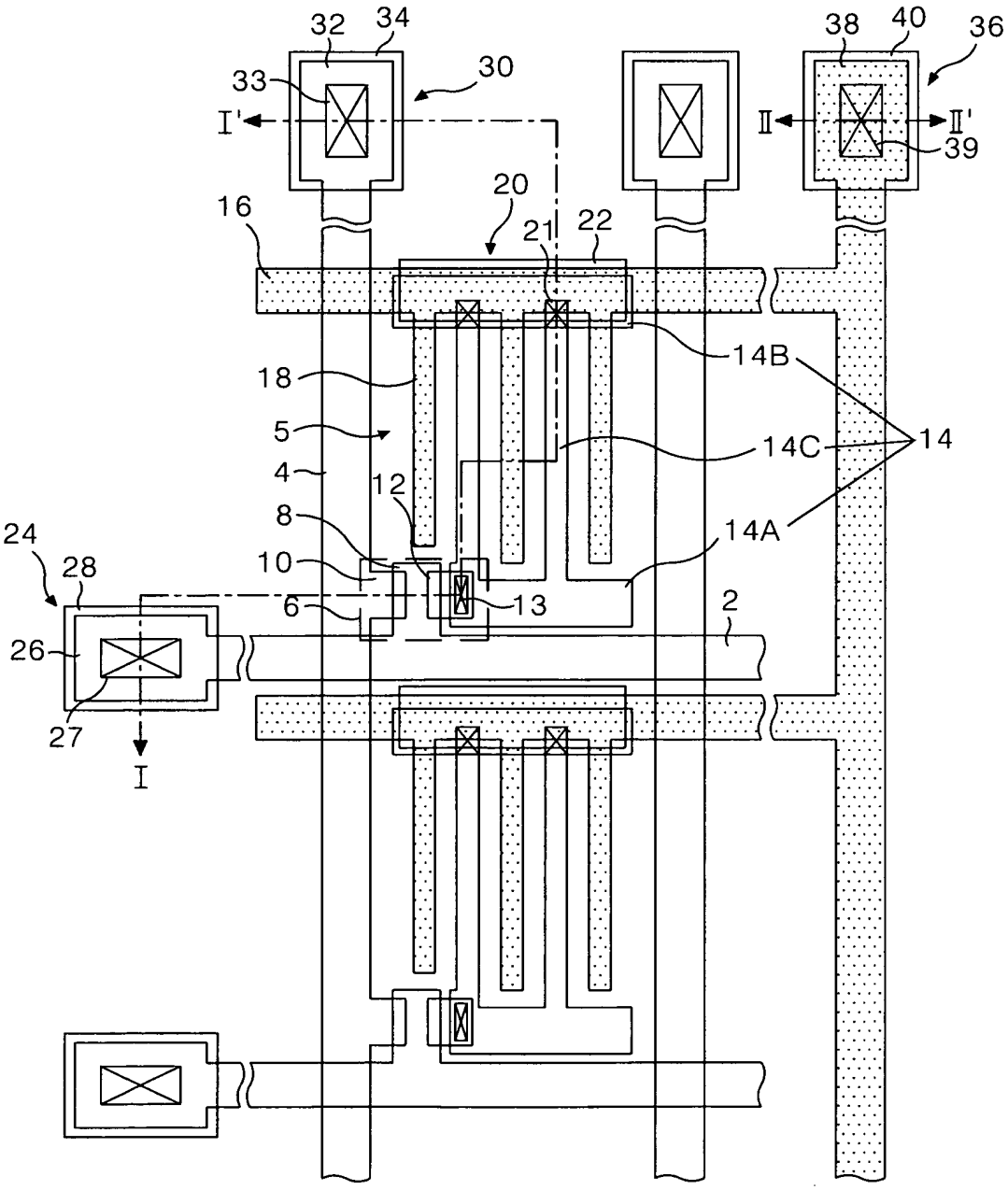
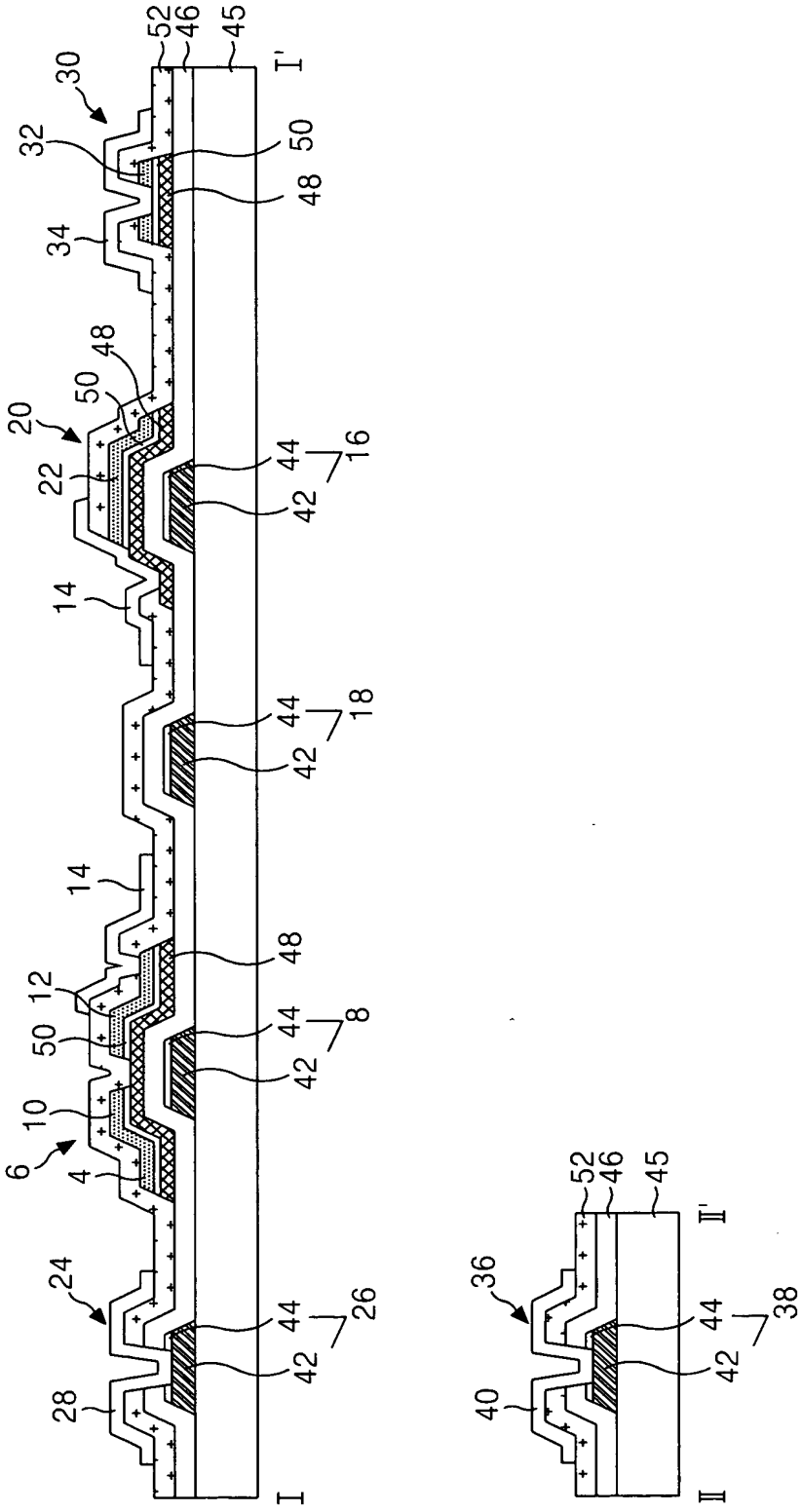


FIG.2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40
II

FIG.3A

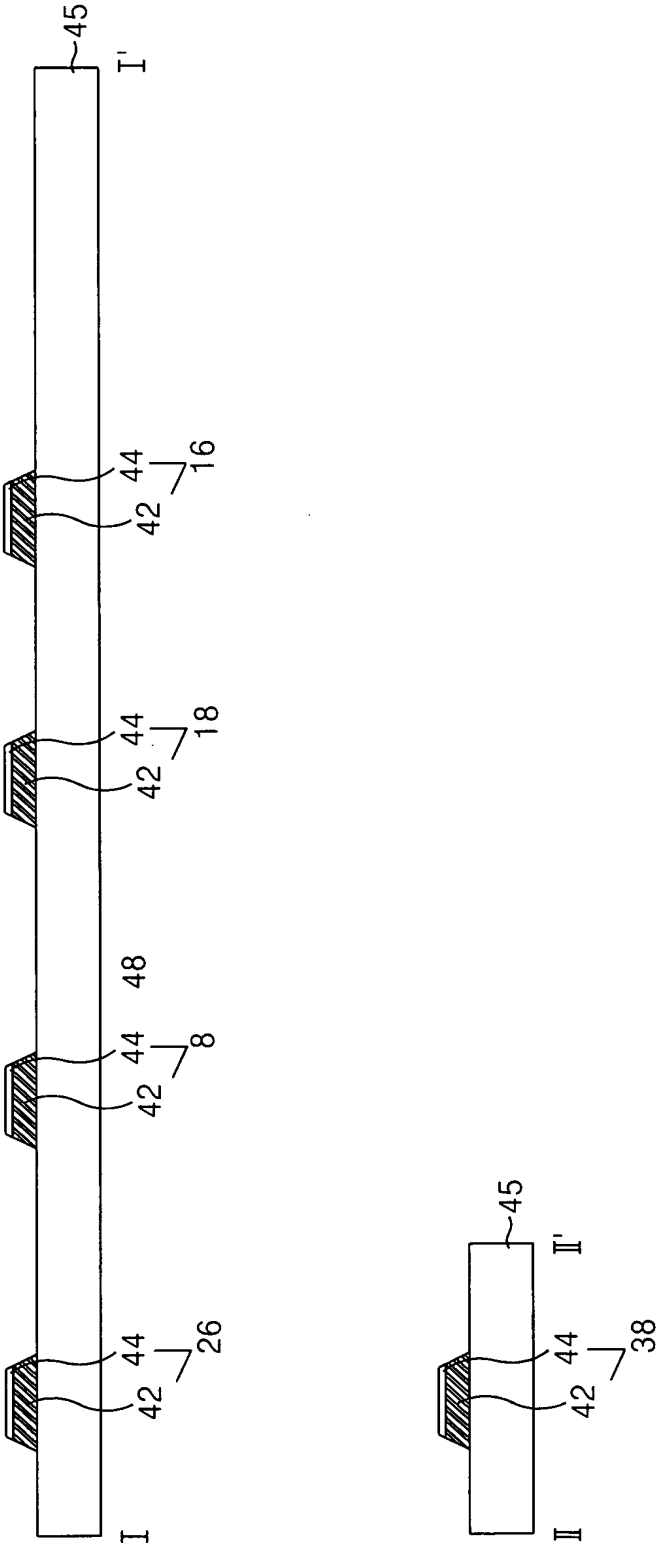
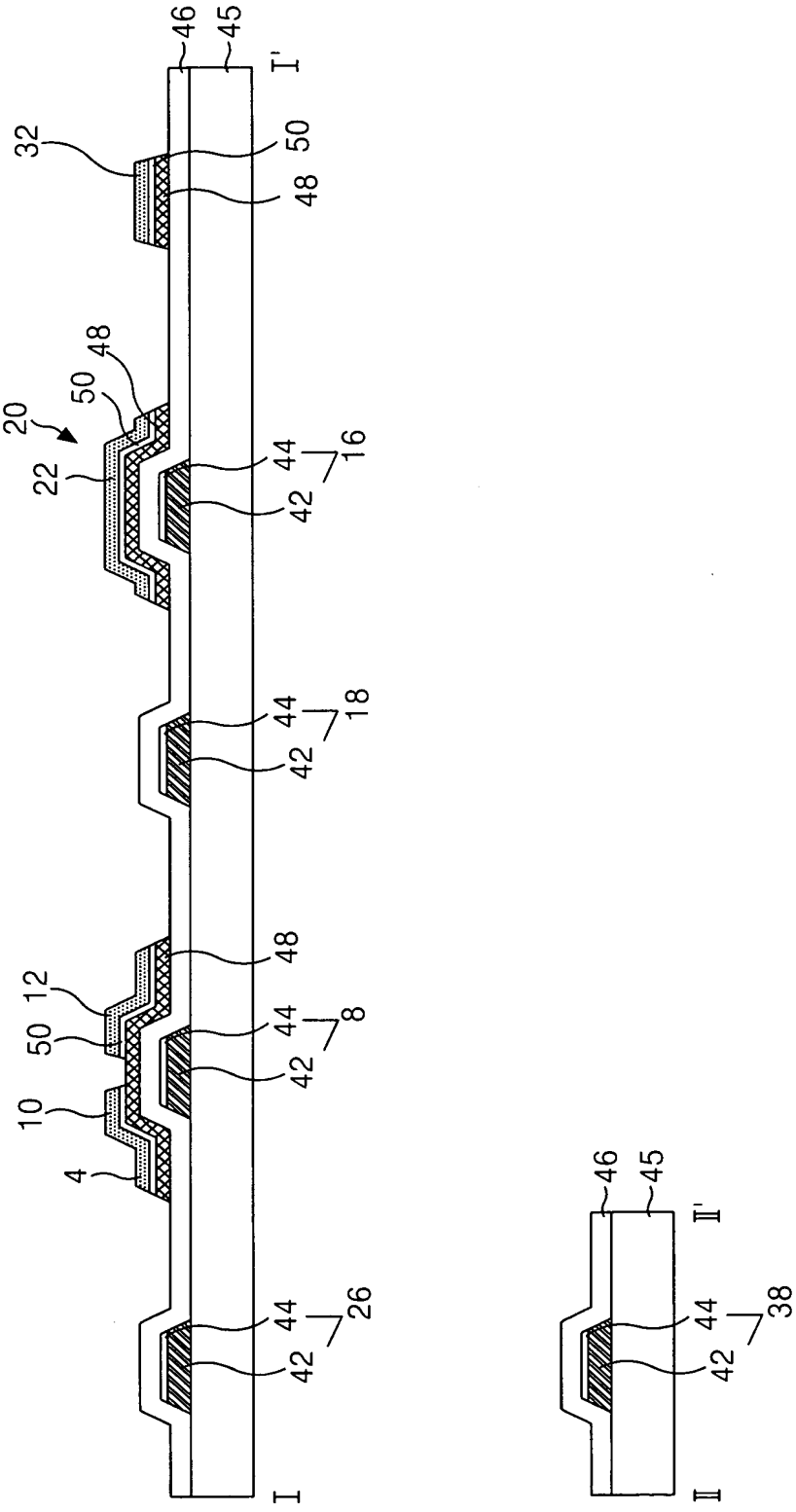


FIG.3B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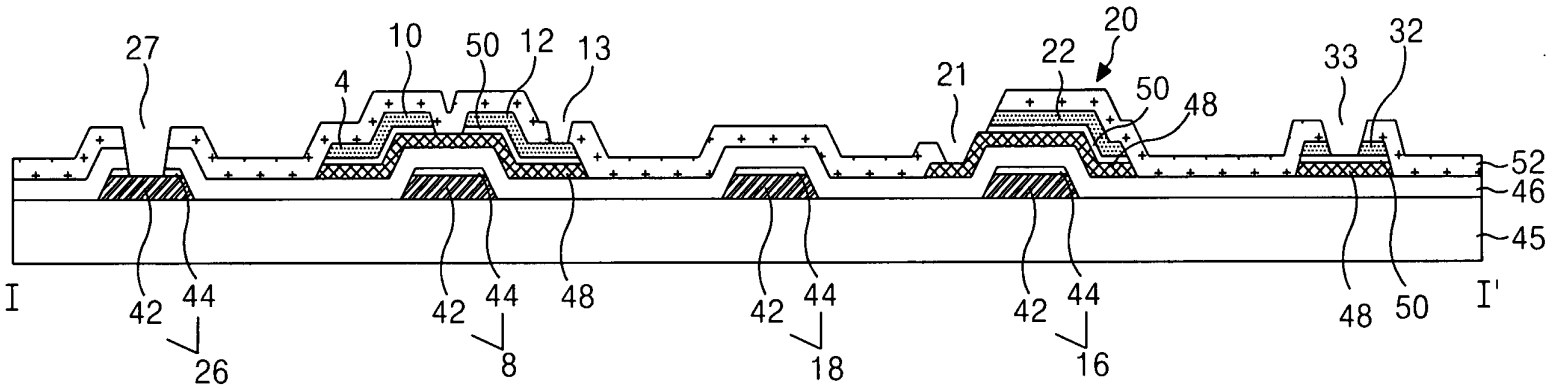
38
42
II

FIG.3C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I'
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18
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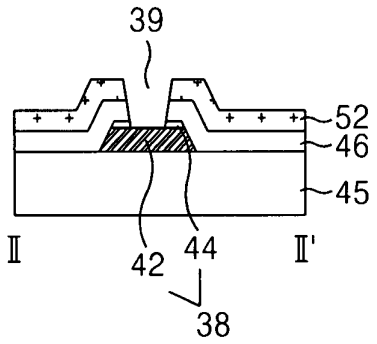
39
52
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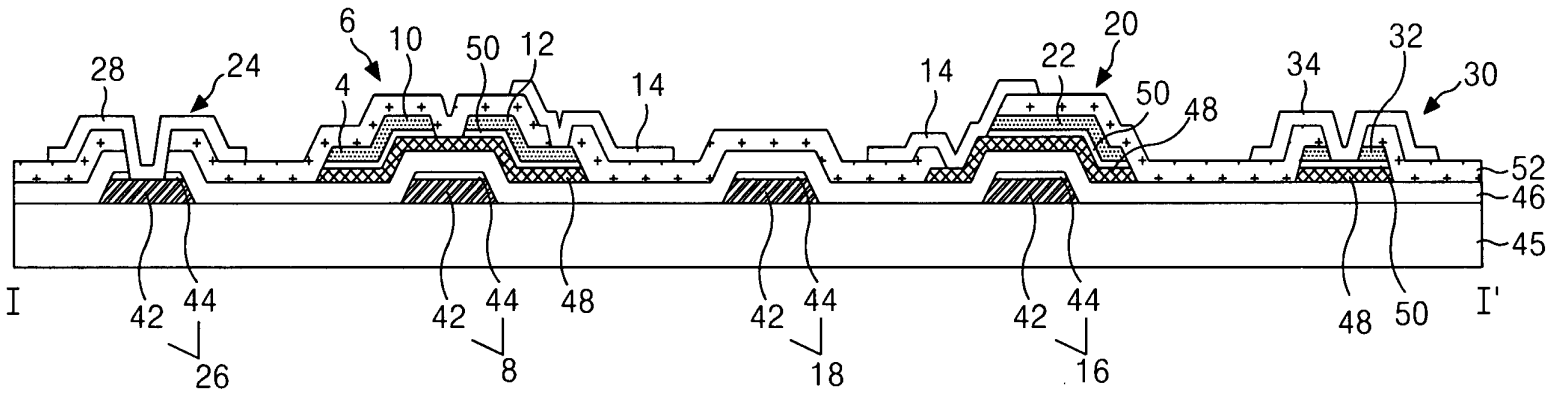
45
II
42
44
II'
38

FIG.3D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50
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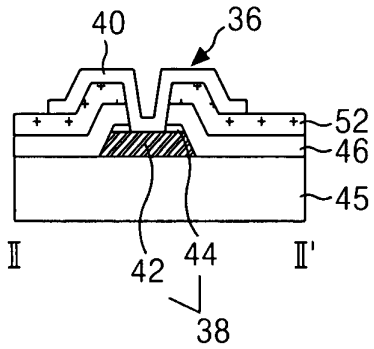
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II
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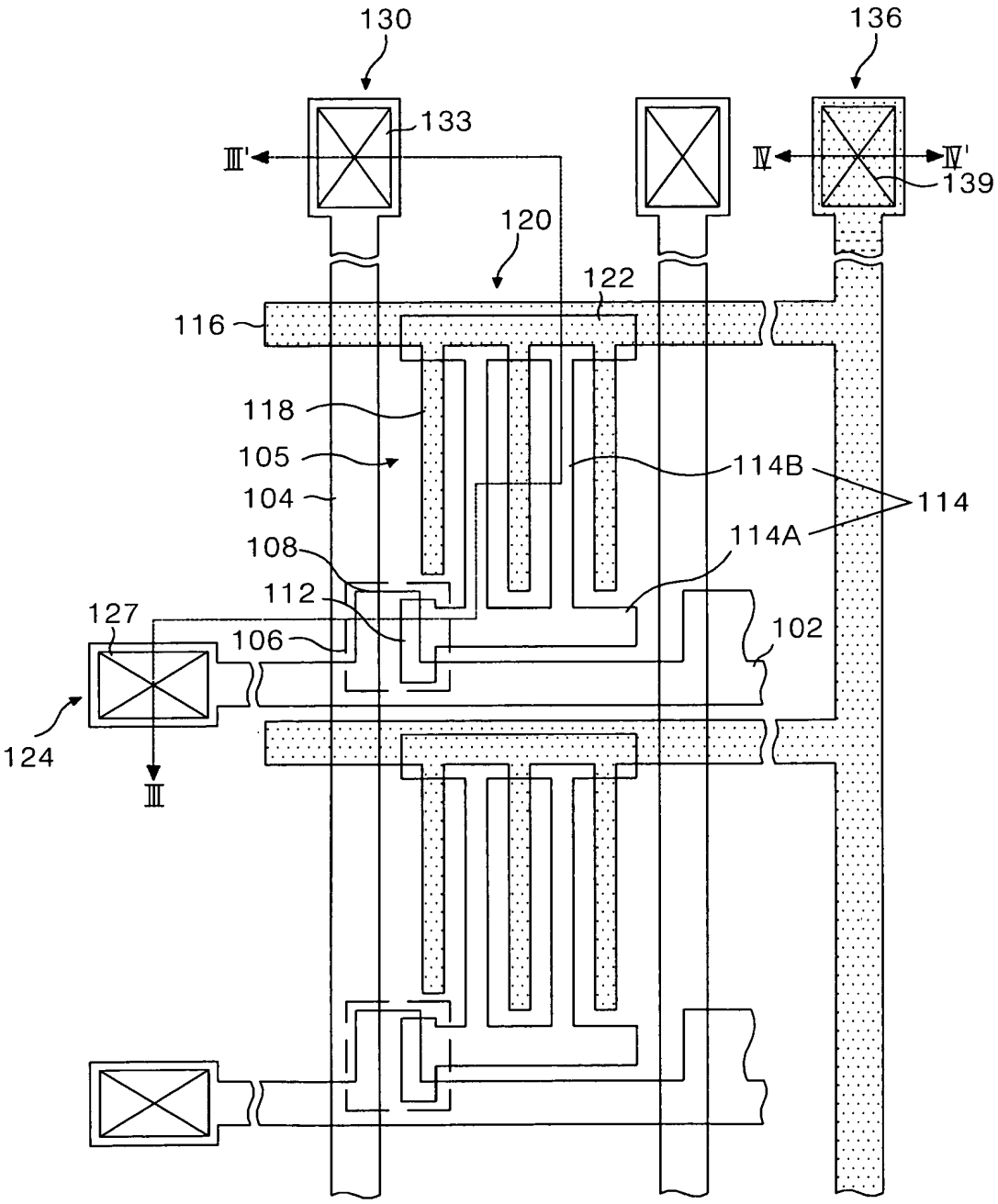
II'

FIG. 4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Ⅳ
Ⅳ'
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114B
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114A
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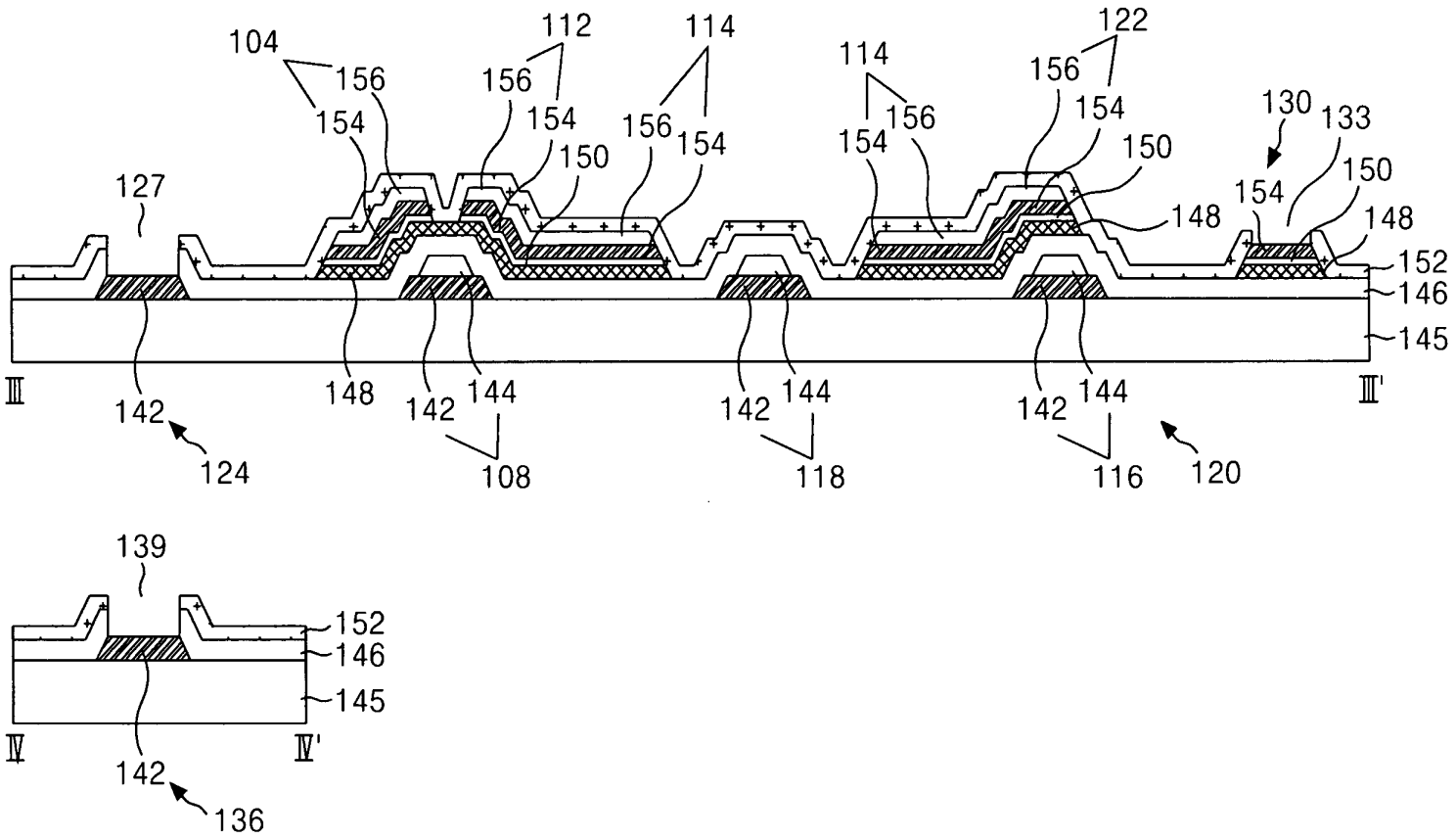
102
124
Ⅲ

FIG.5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136

FIG.6A

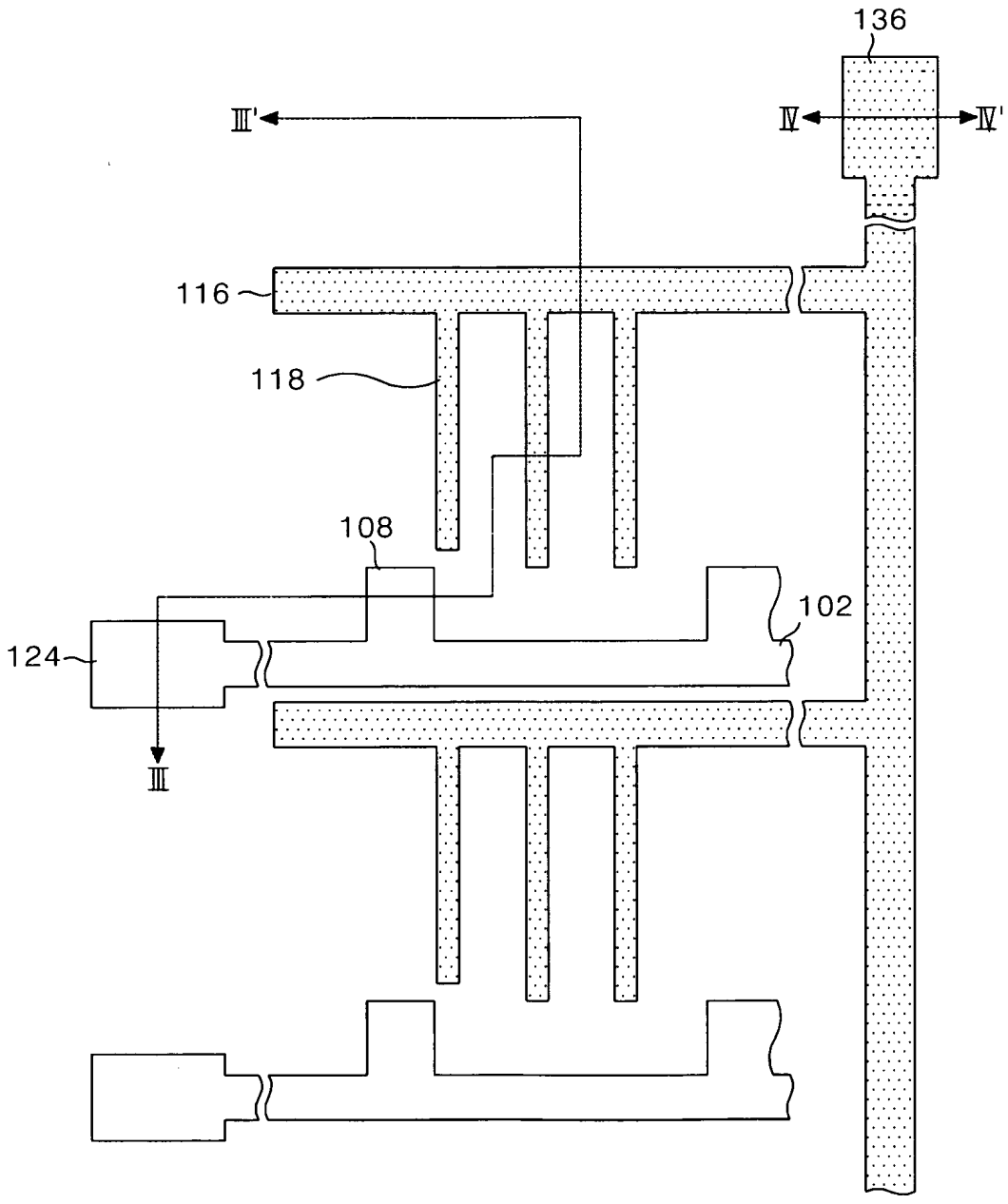
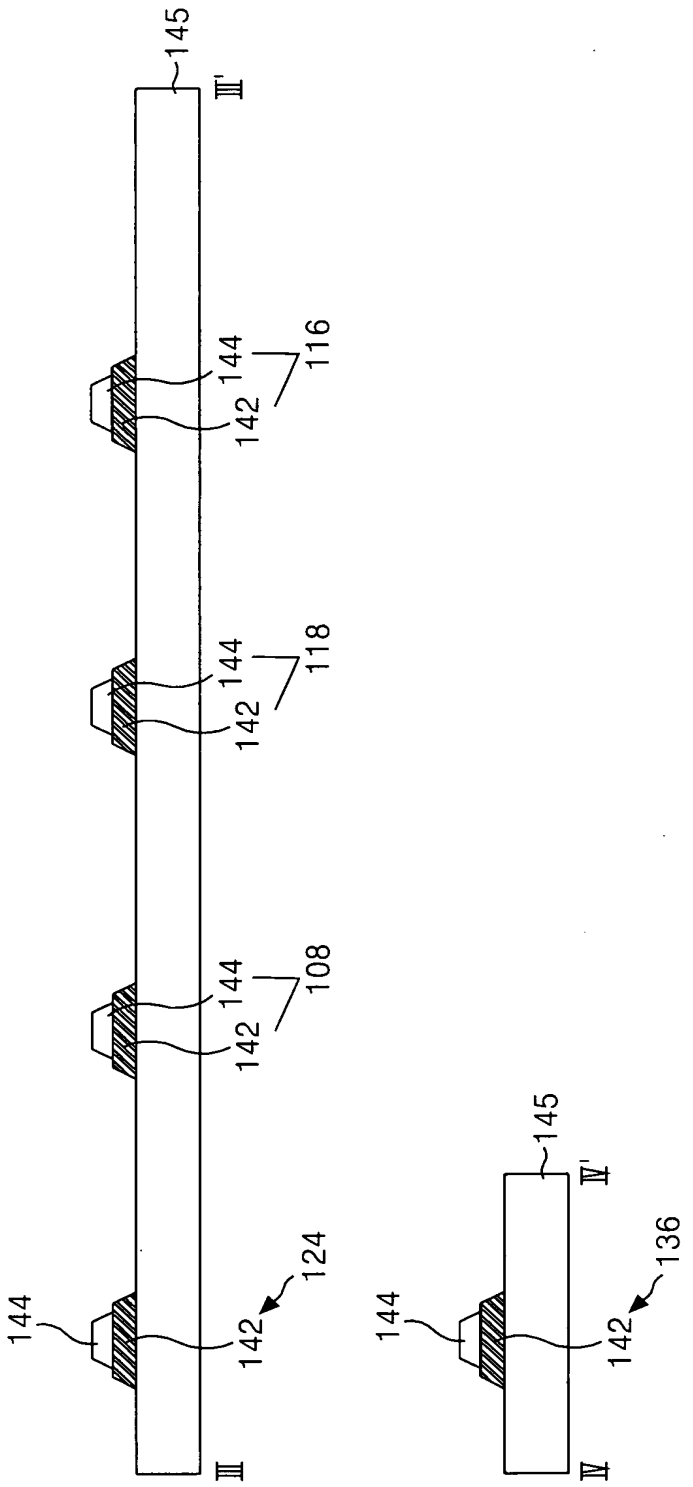


FIG.6B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144
142
118
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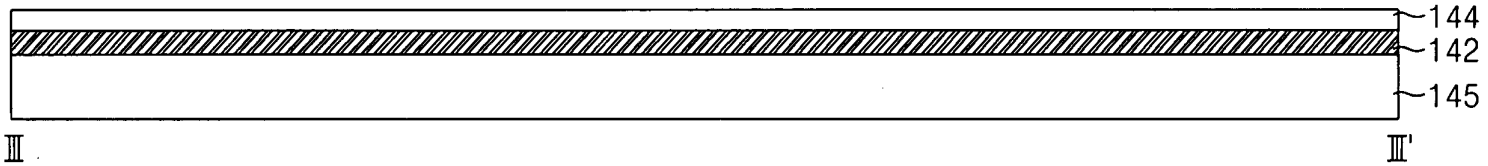
142
124
144
142
Ⅲ
145
Ⅳ'
136
144
142
Ⅳ

FIG.7A



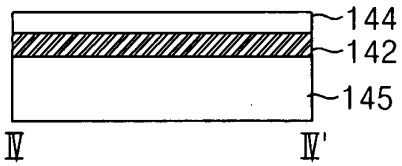
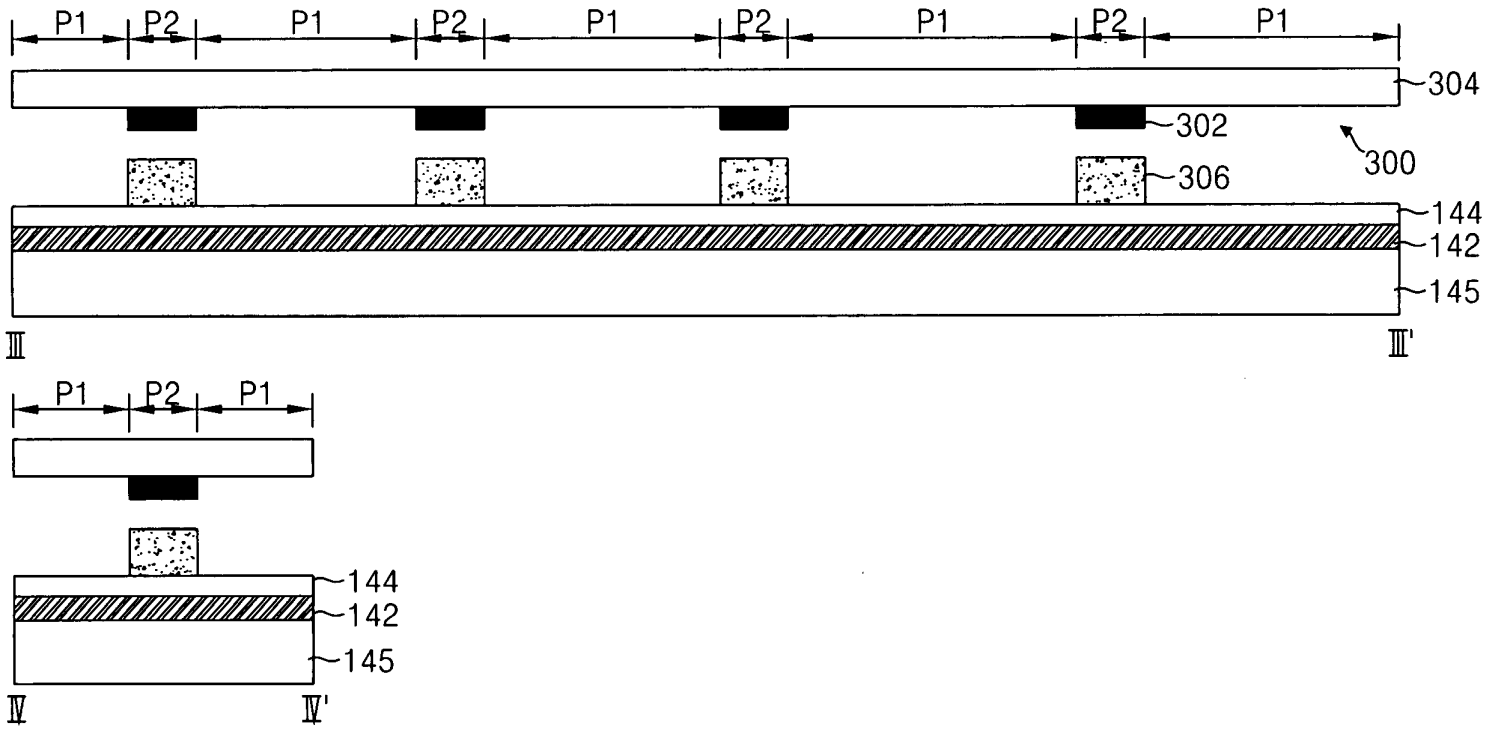


FIG.7B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P2
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P2
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P2
P1
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302
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306
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142
145
Ⅲ
Ⅲ'
P1
P2
P1
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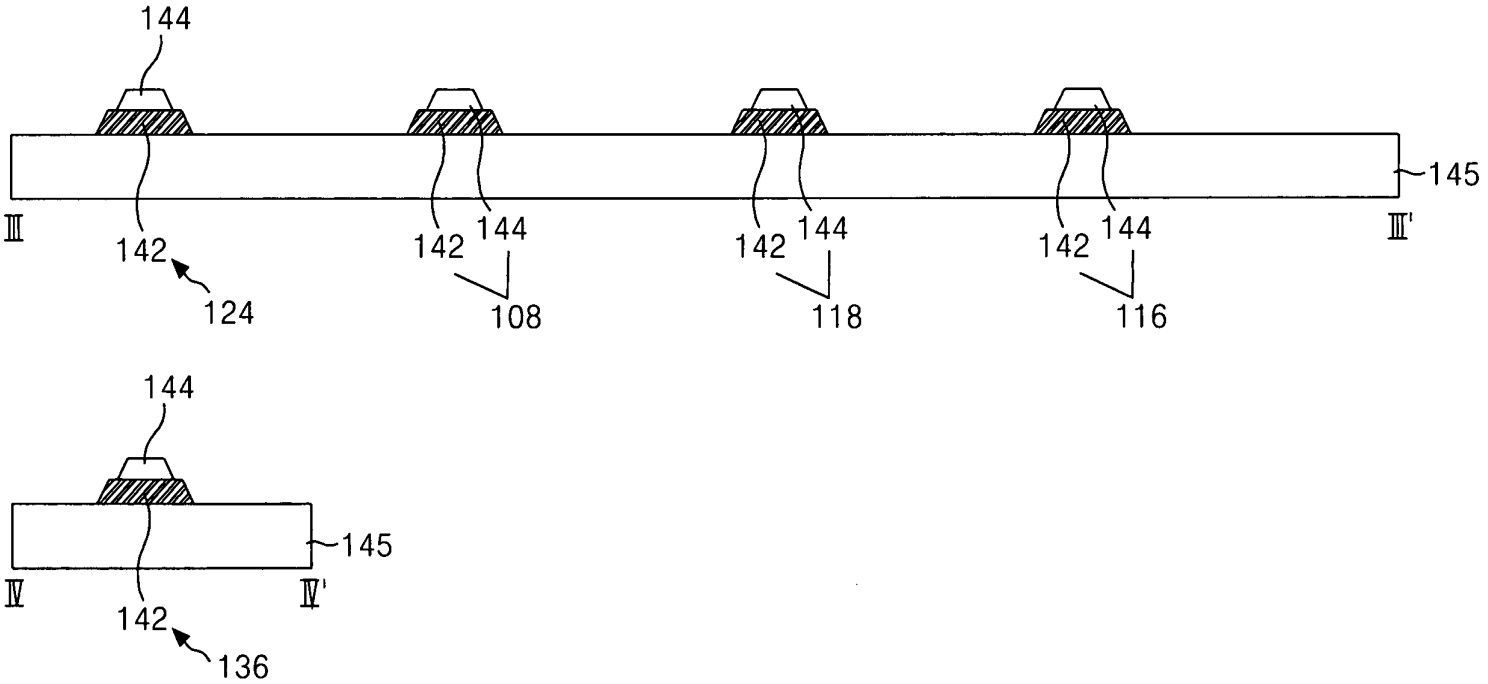
Ⅳ'

FIG.7C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Ⅲ'
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Ⅳ'
142
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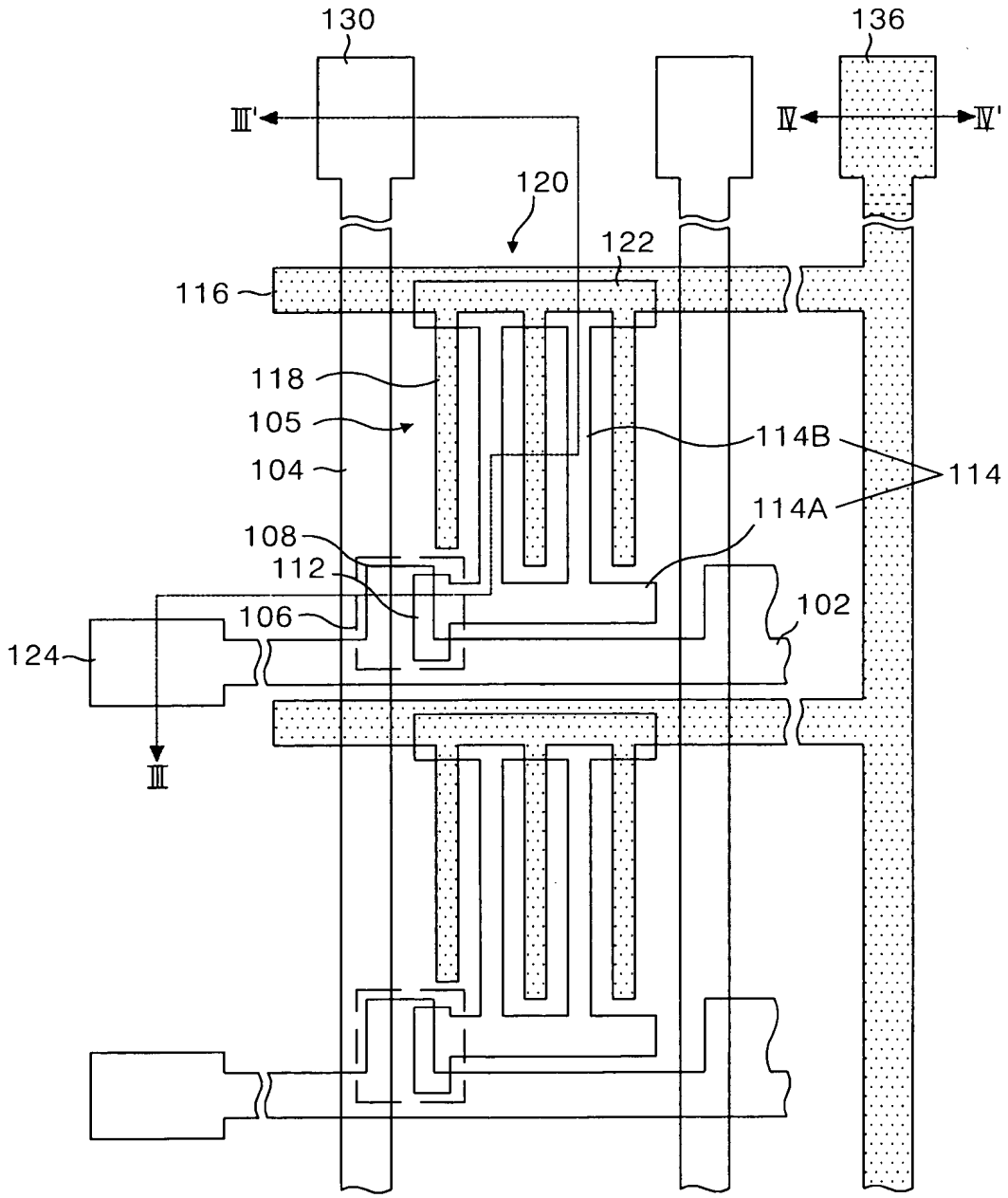
FIG.8A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114B
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114A
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Ⅲ

FIG.8B

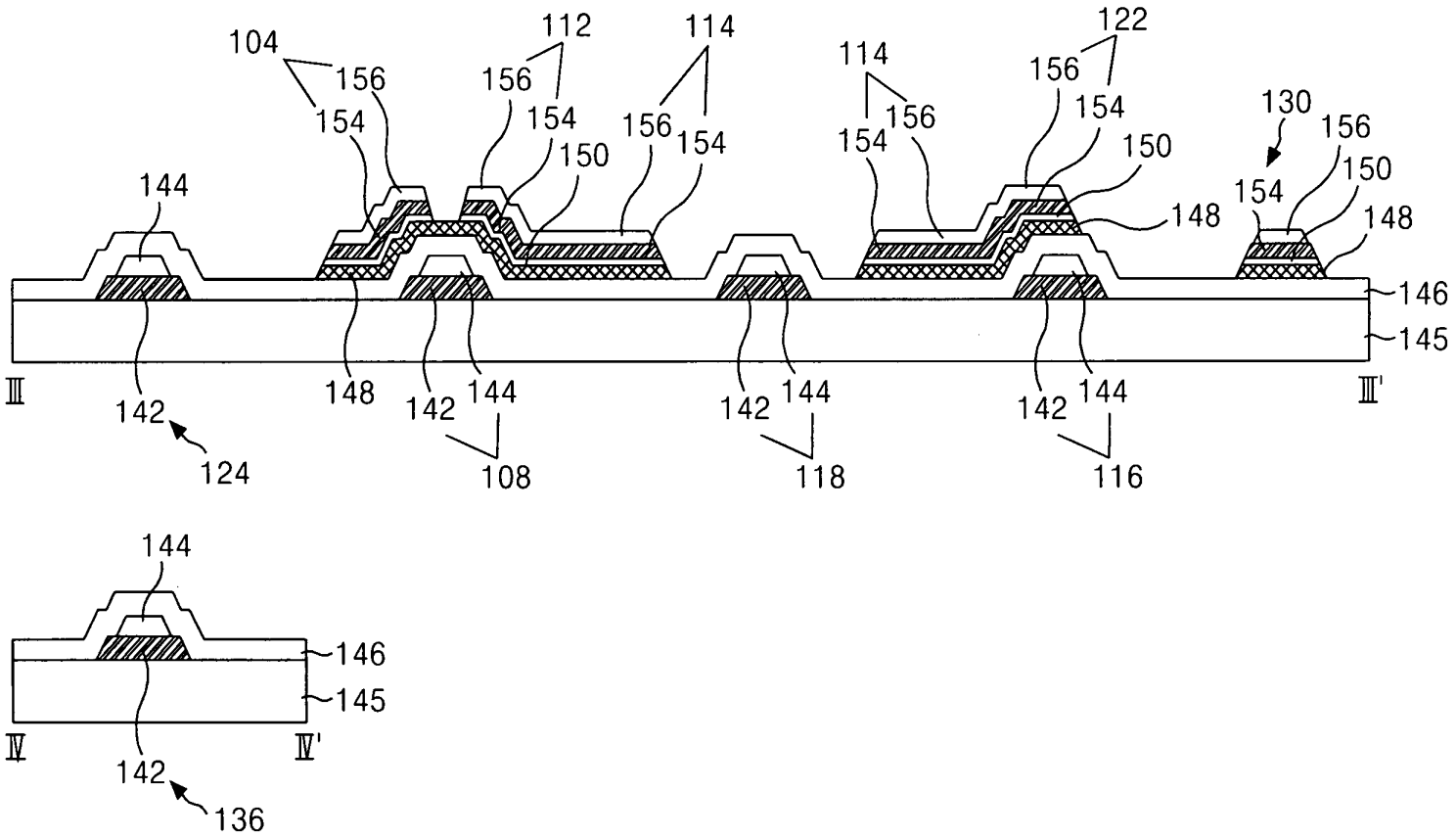
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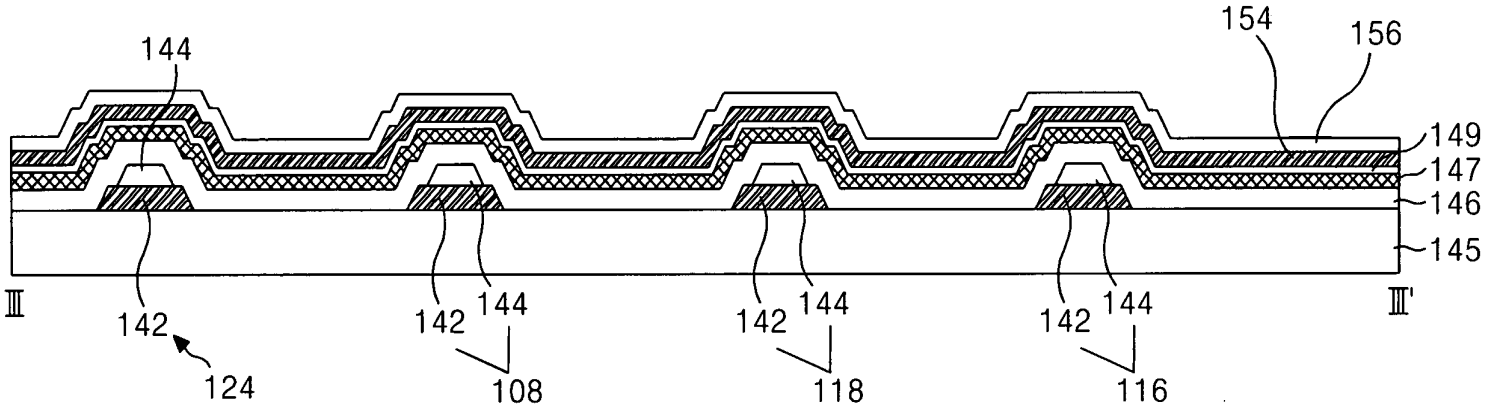
FIG.9A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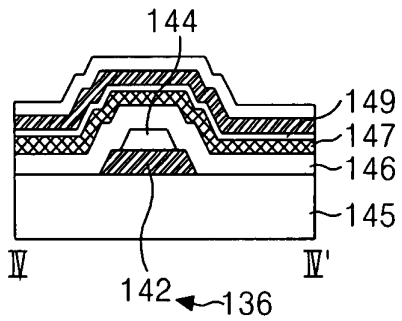
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Ⅳ
Ⅳ'
142
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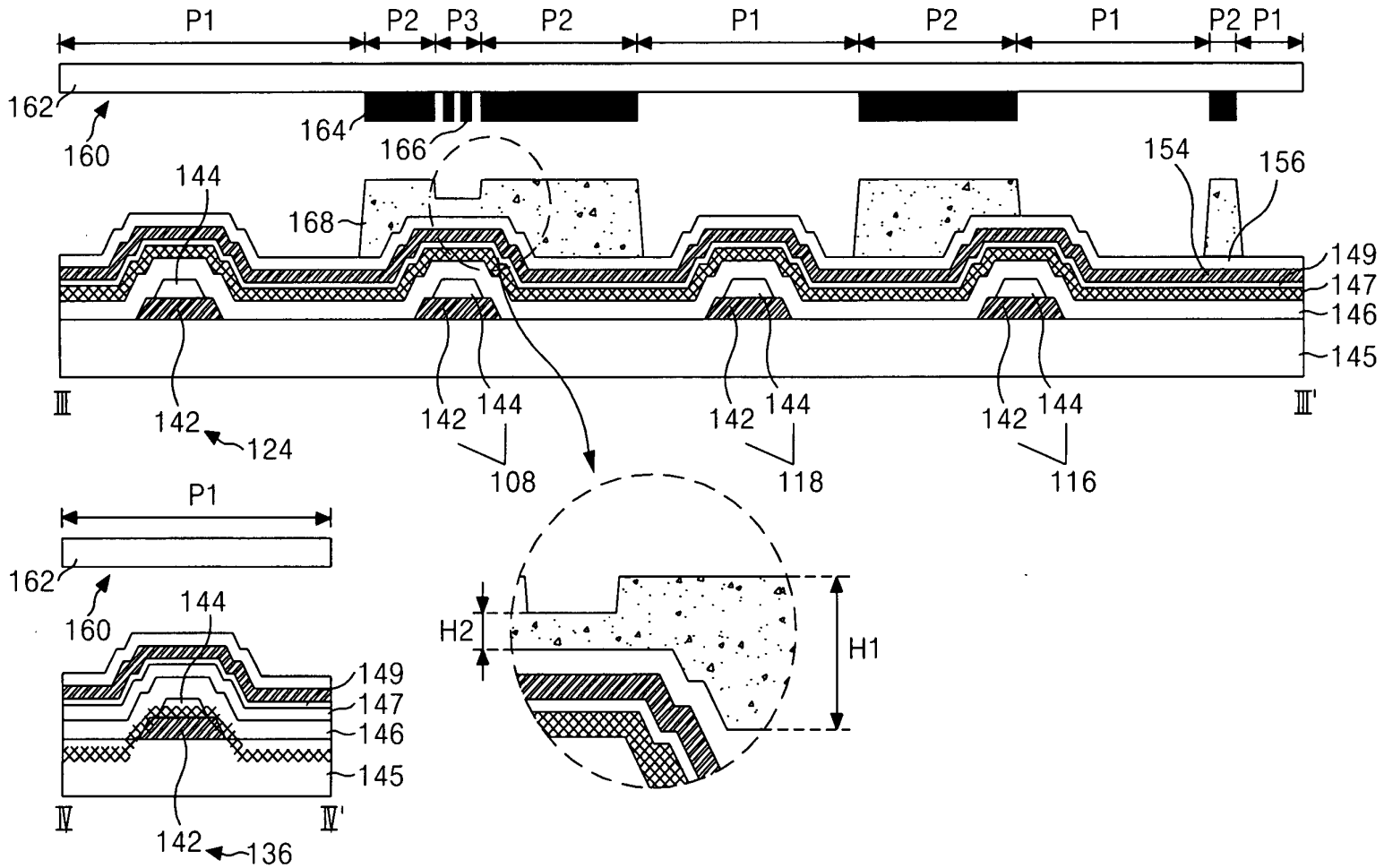
FIG.9B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142
136
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H2
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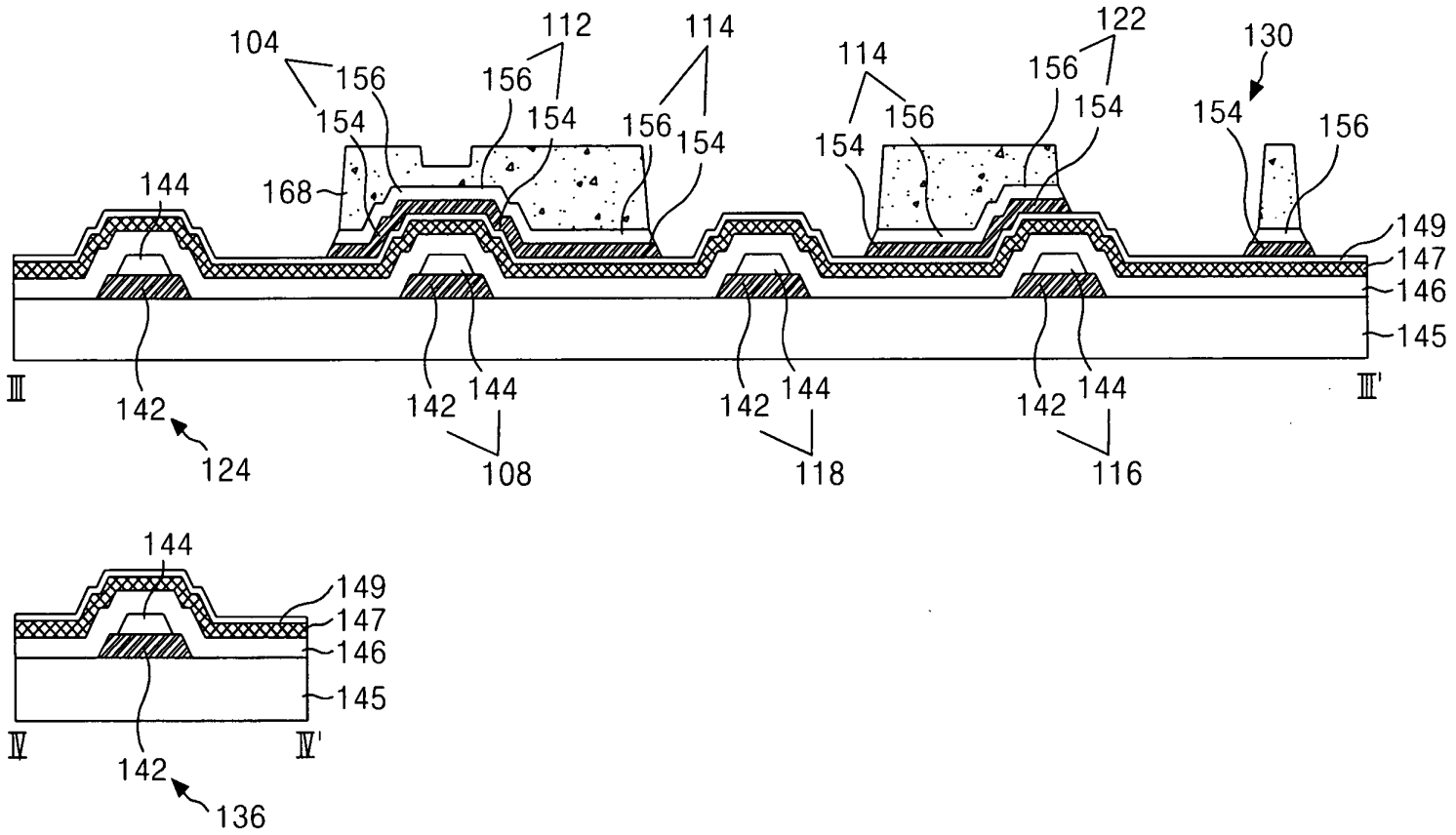
FIG.9C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Ⅳ
Ⅳ'
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FIG.9D

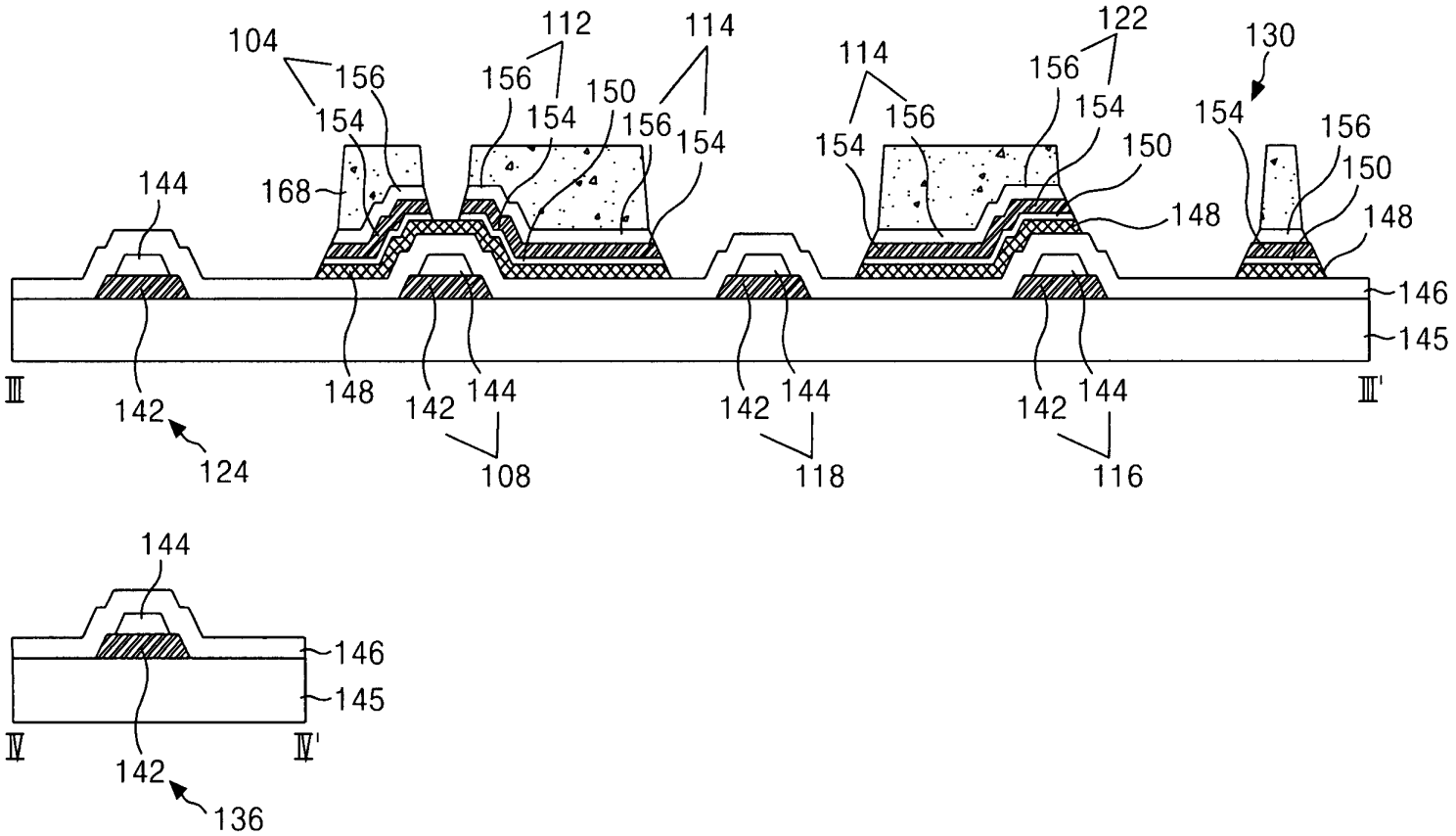
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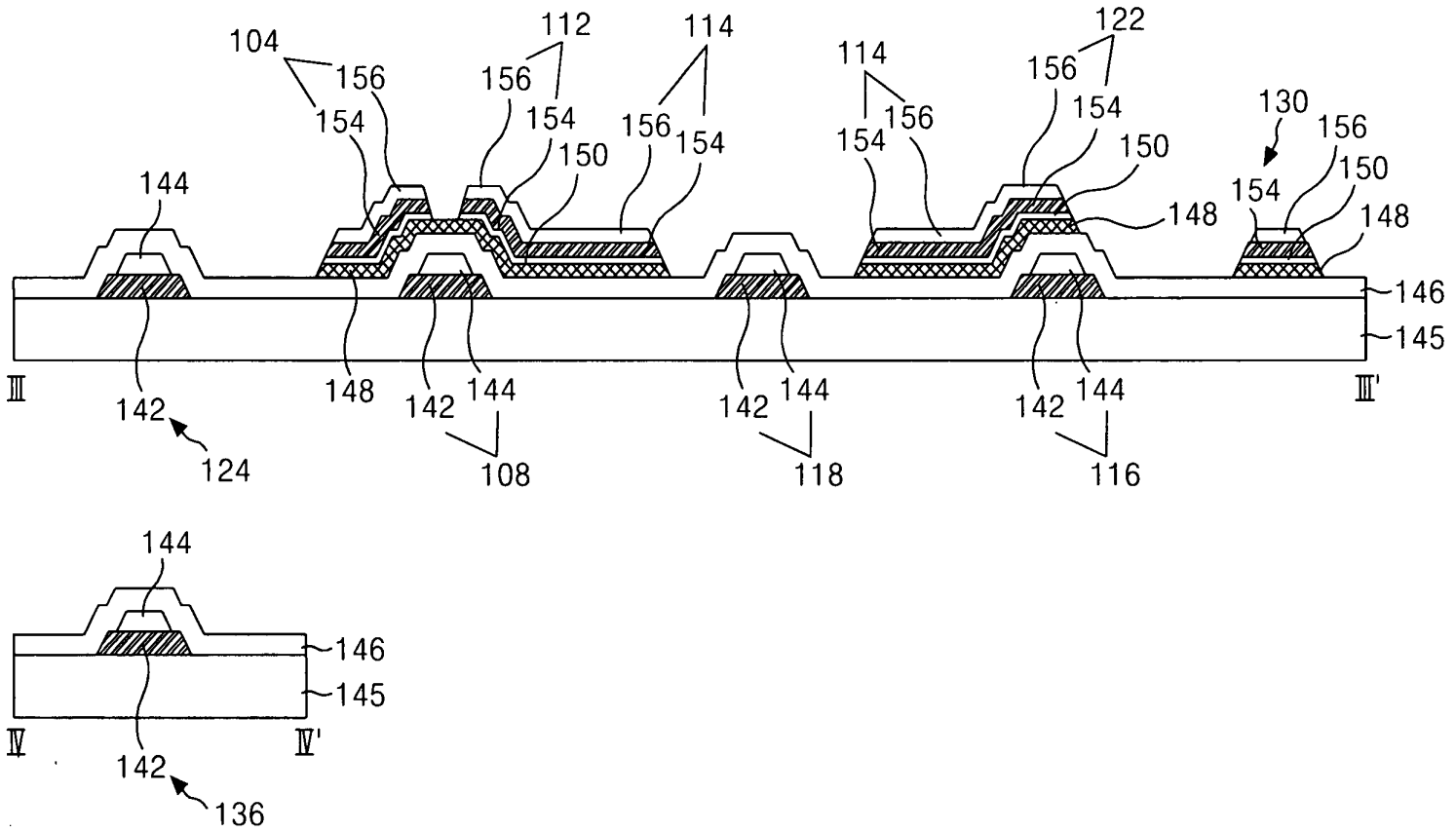
FIG.9E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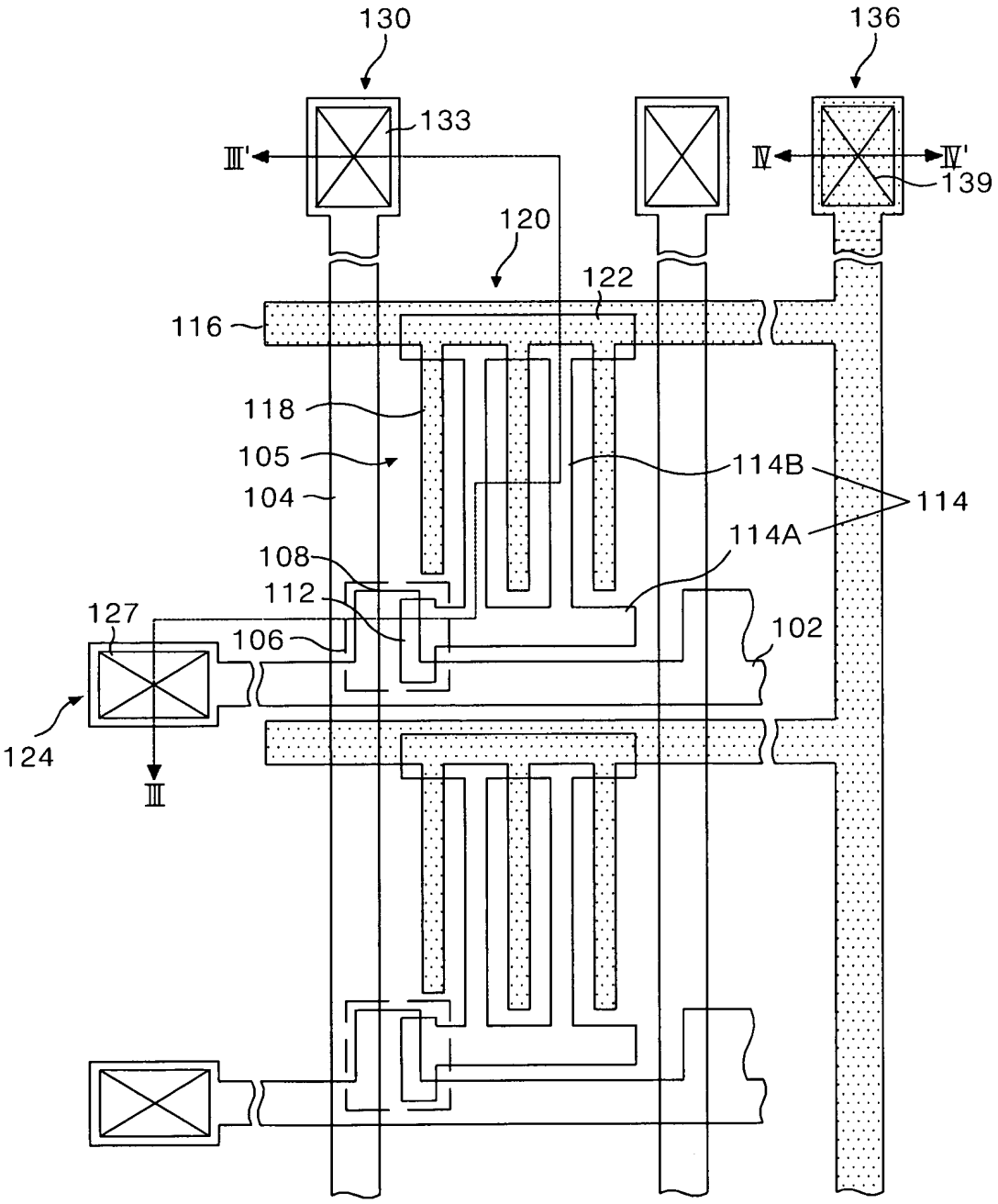
Ⅳ'

FIG.10A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124
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FIG.10B

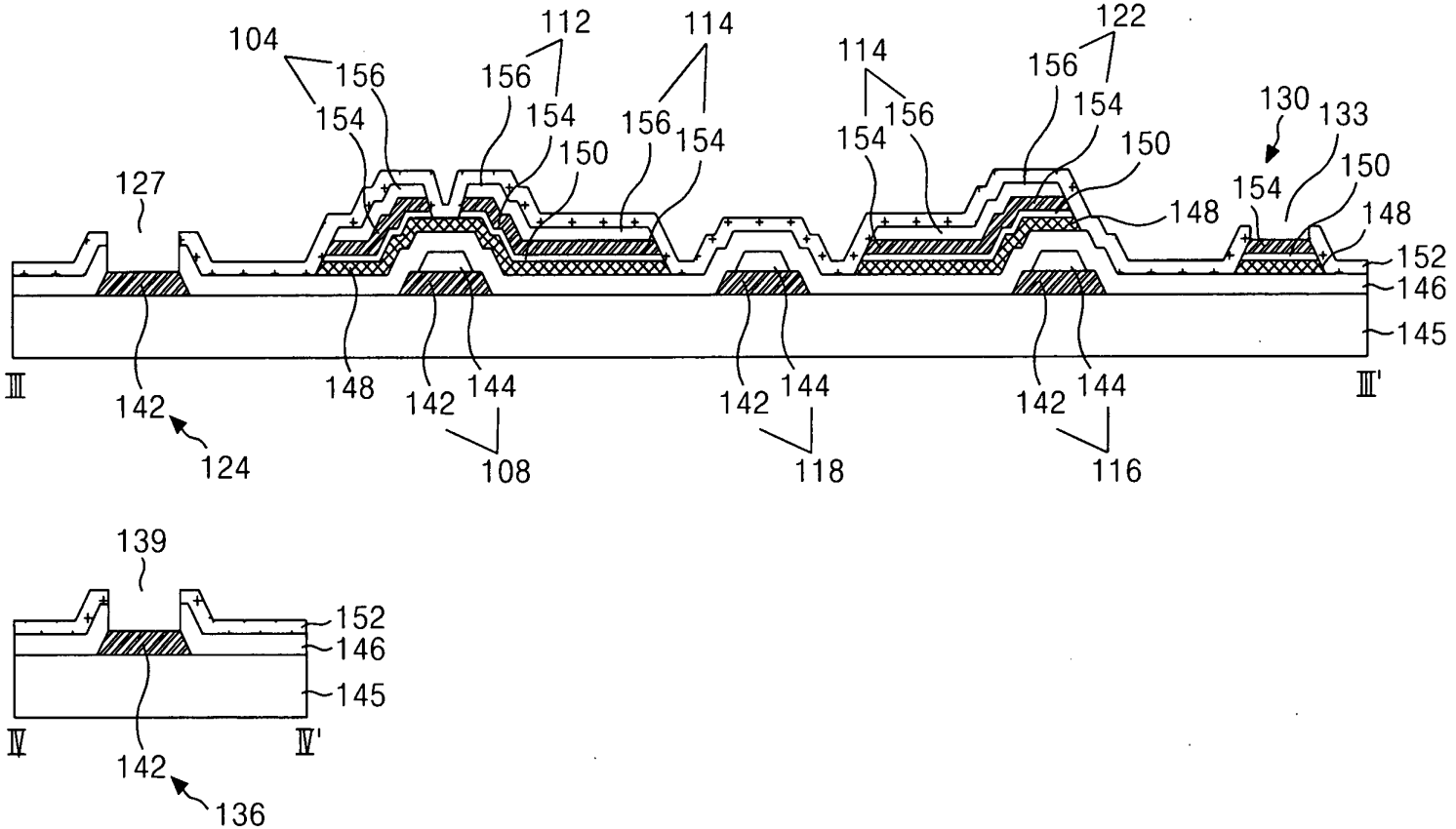
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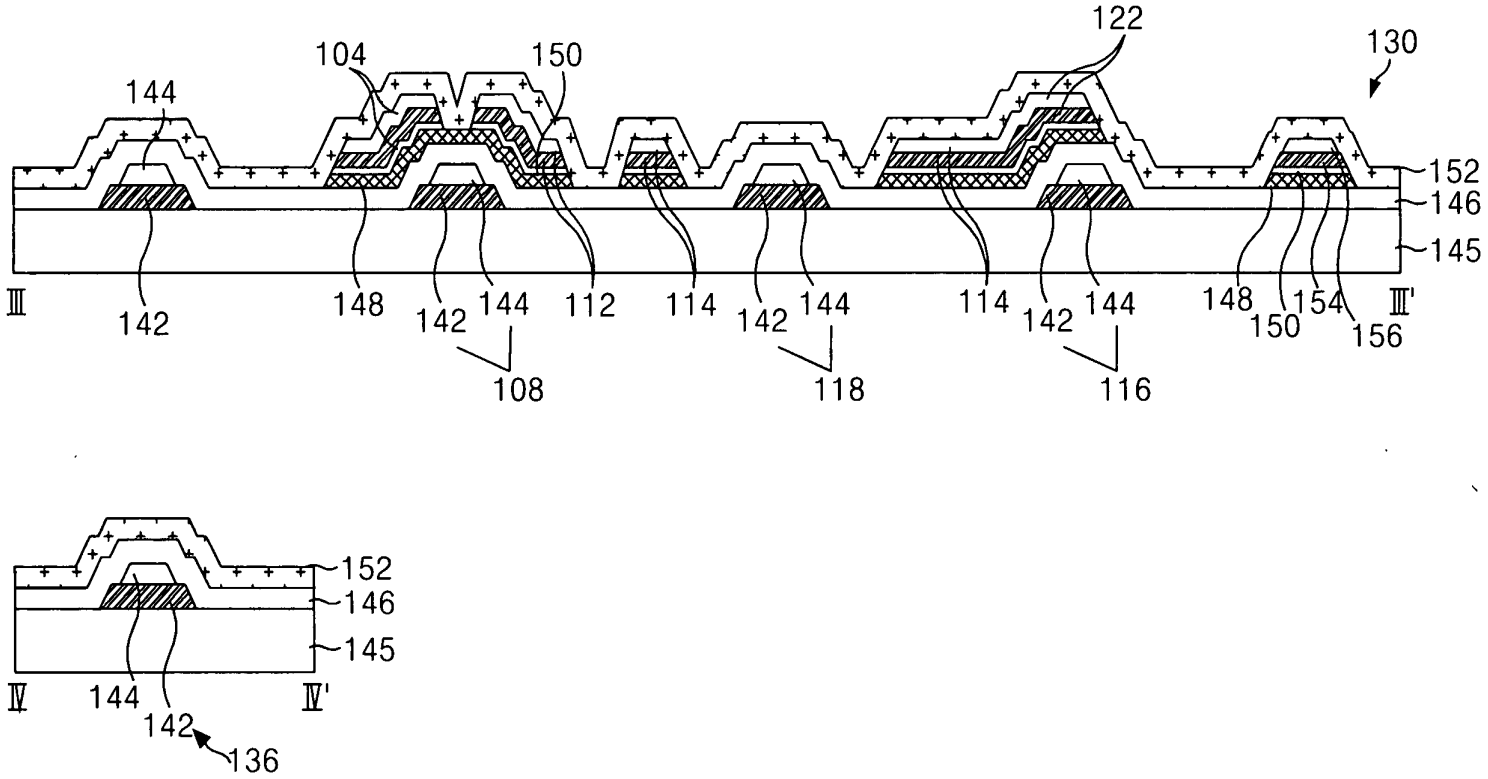
FIG.11A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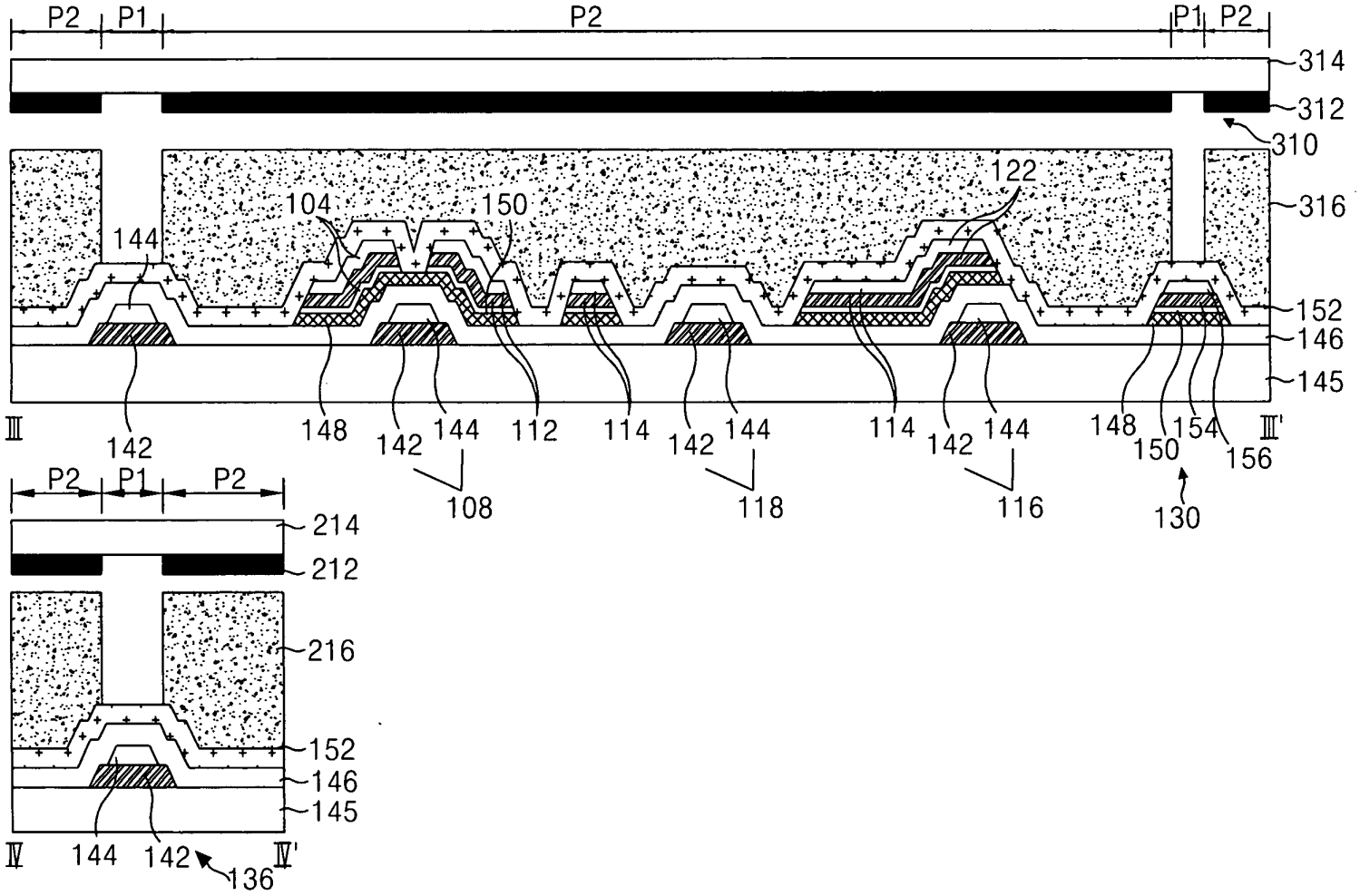
Ⅳ'

FIG.11B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P2
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216
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142
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Ⅳ'

FIG.11C

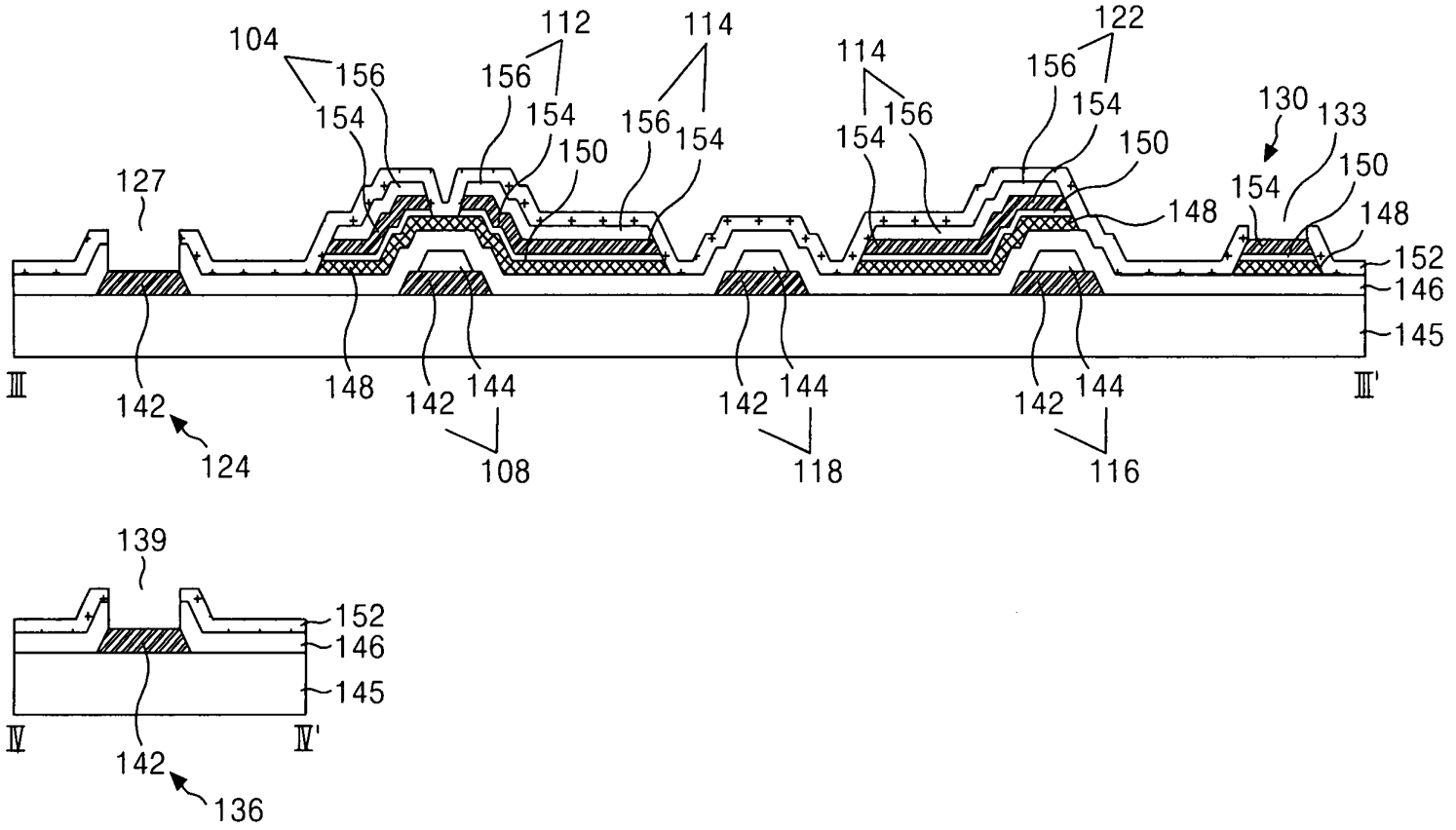
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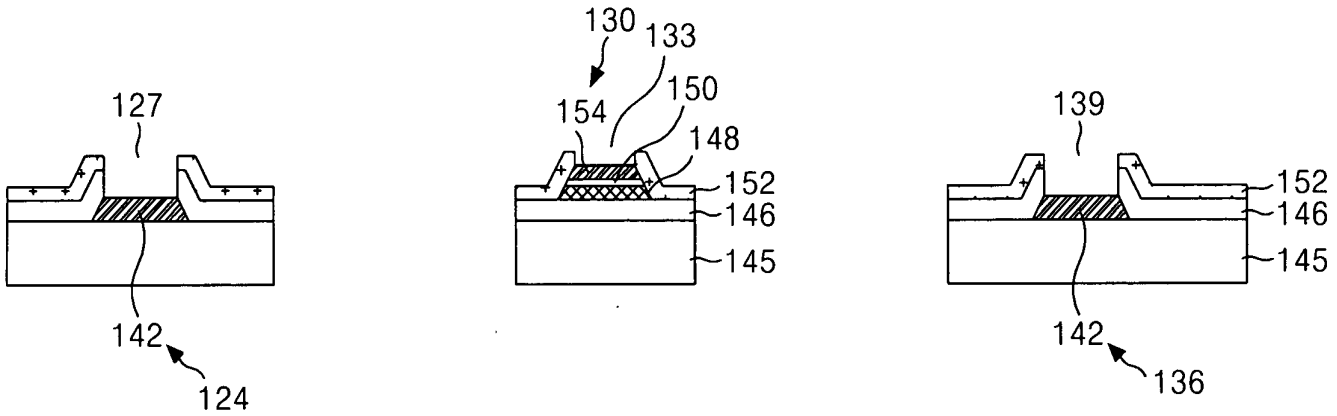
FIG.12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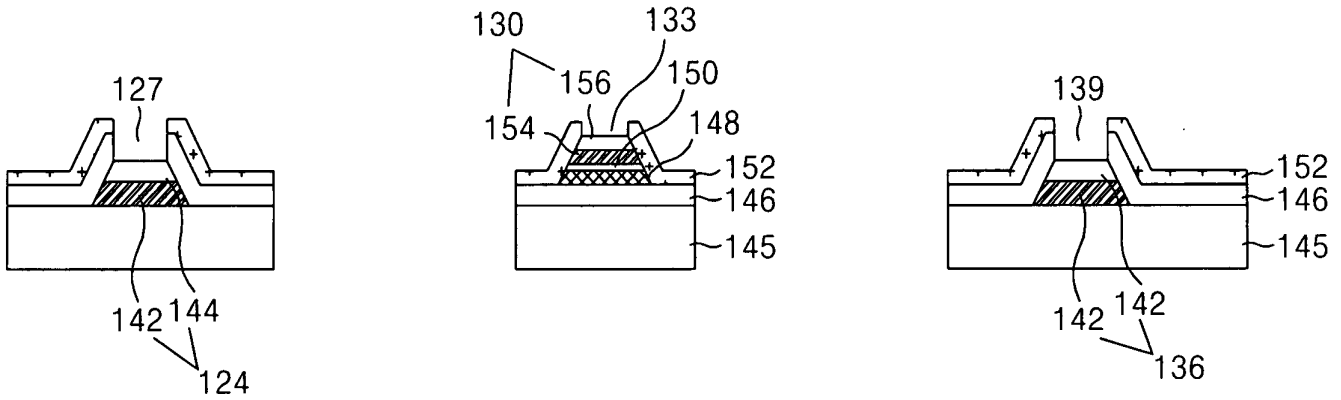
136

FIG.13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136

FIG.14

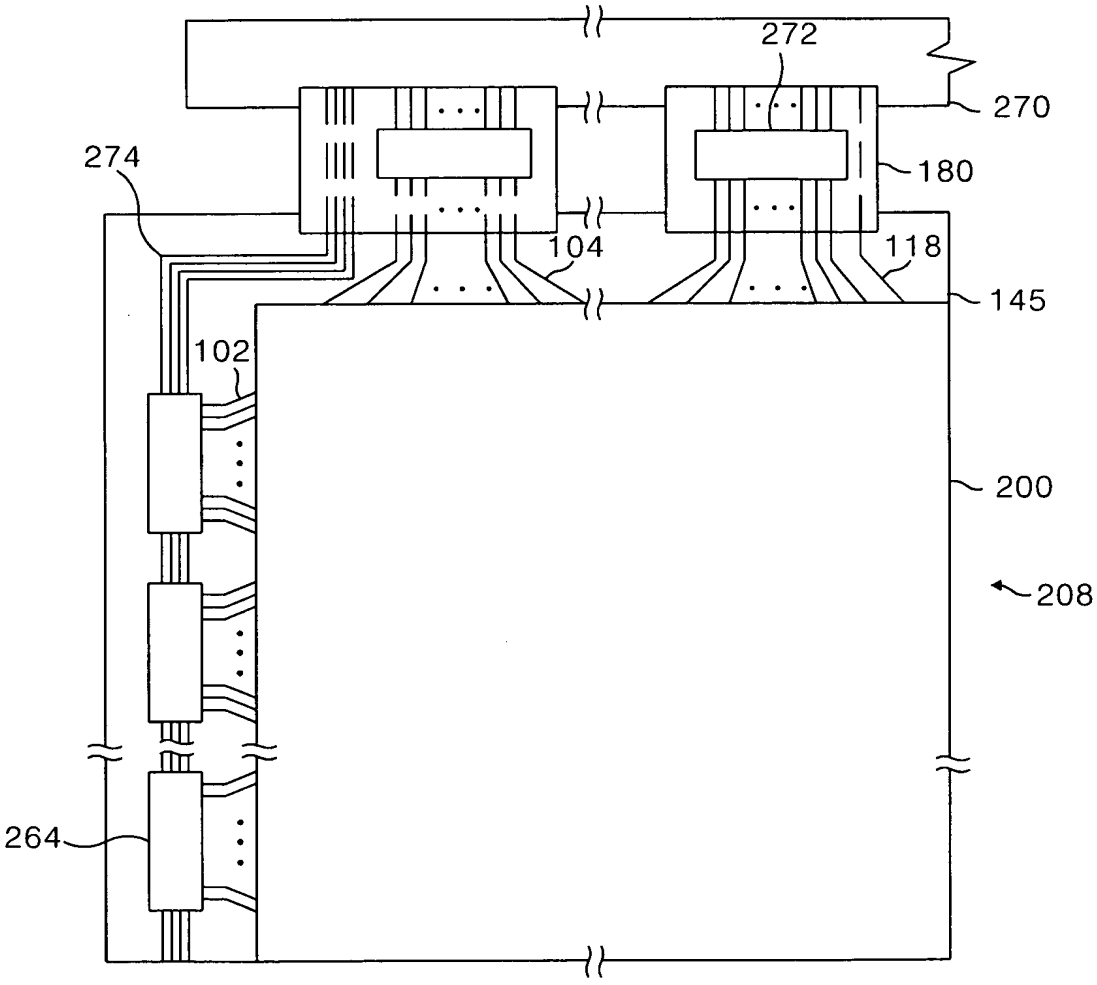
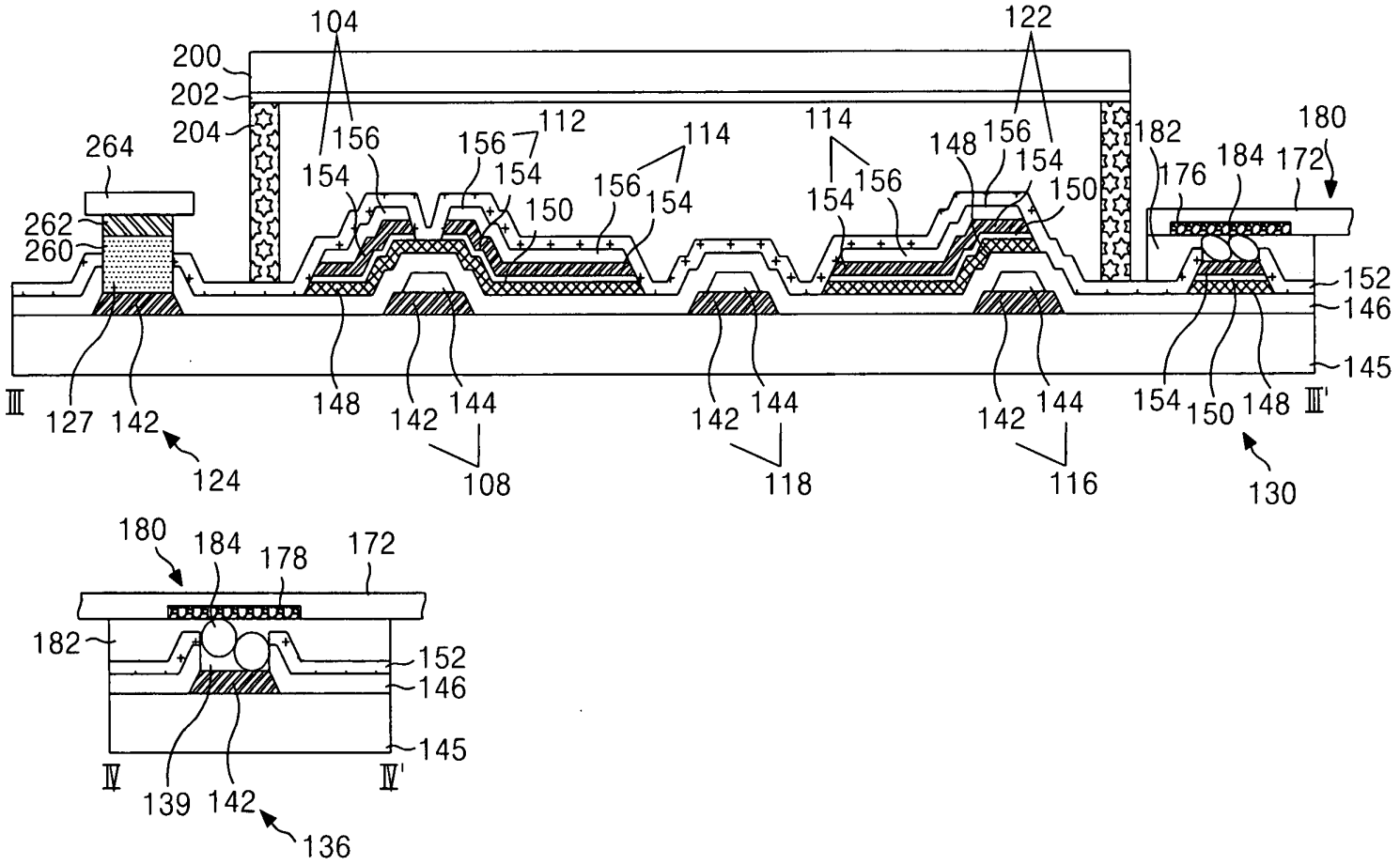


FIG.15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Ⅳ'
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178

FIG.16

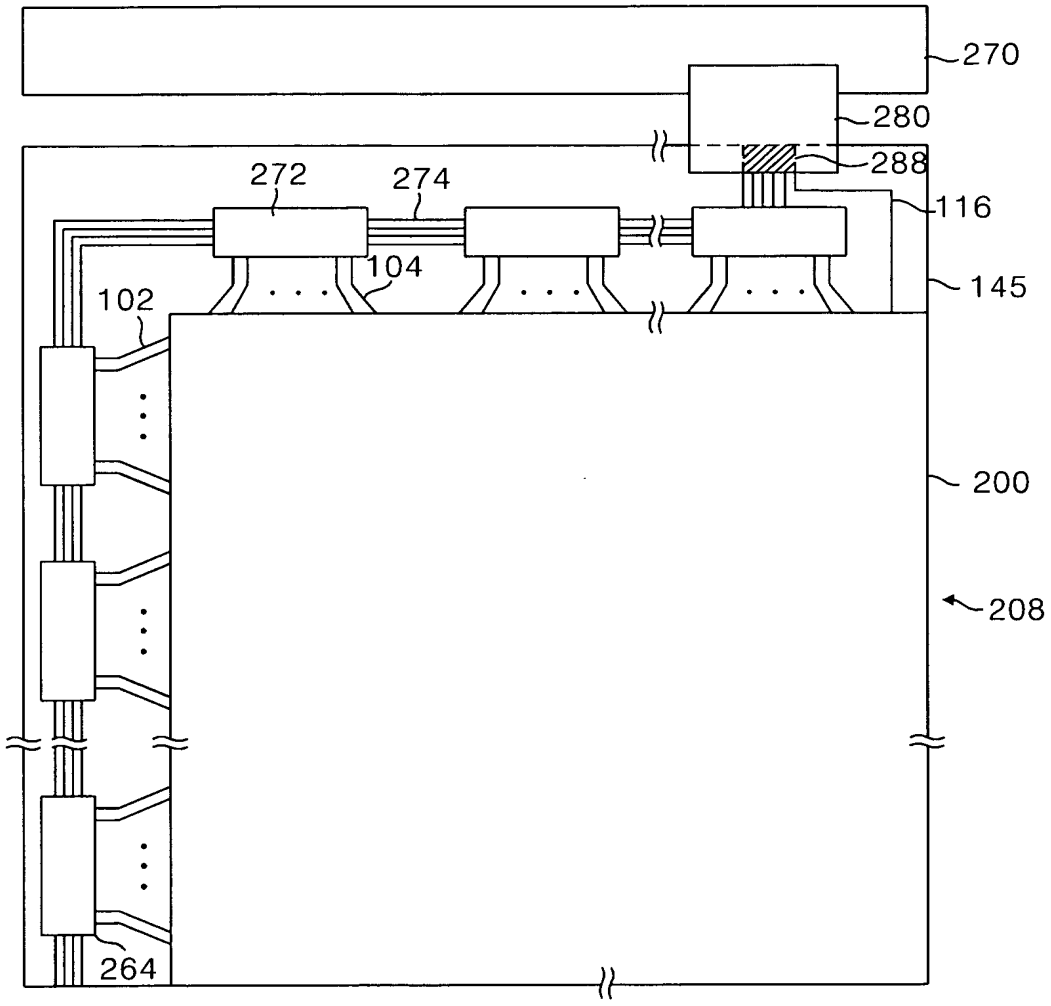
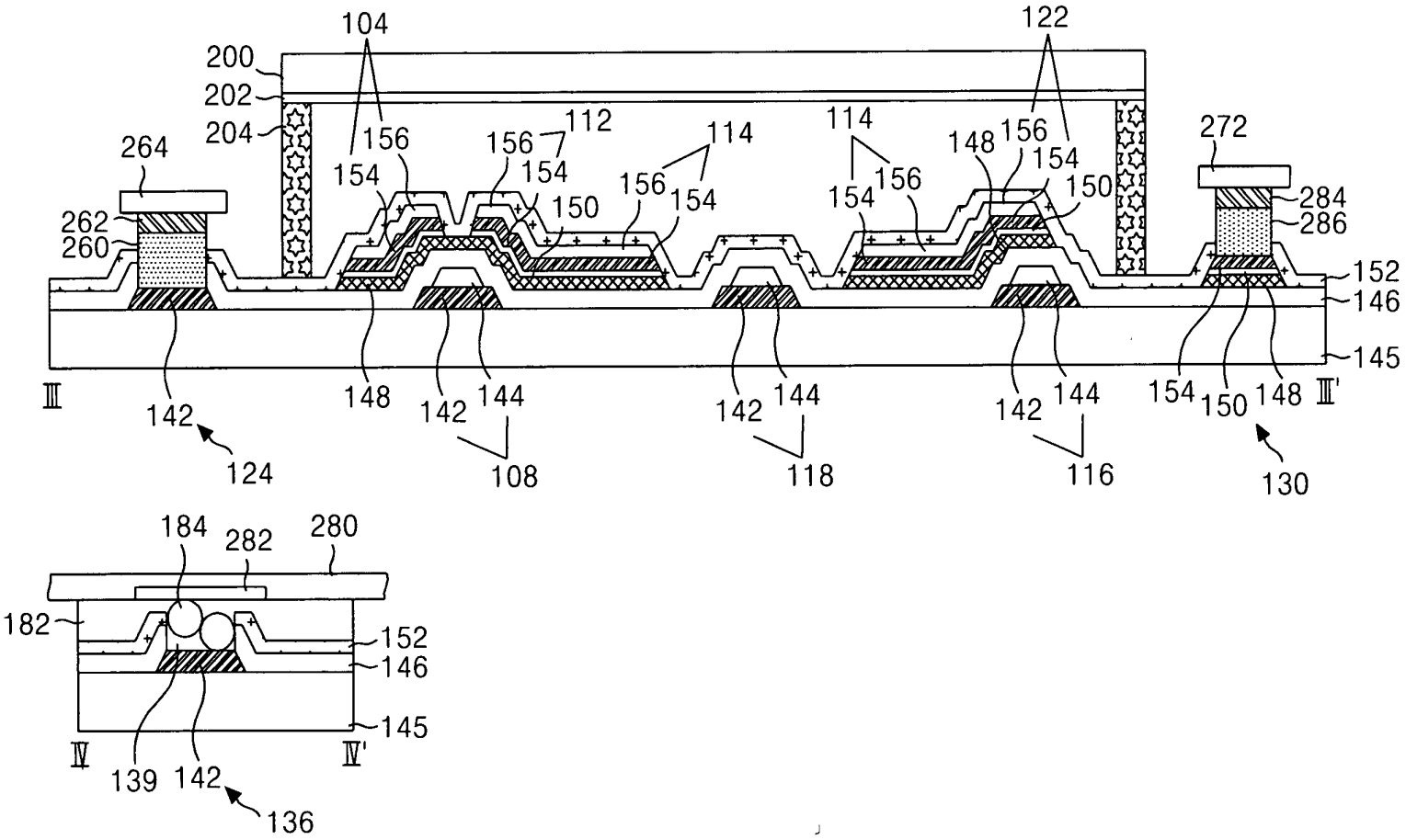


FIG.17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